APPENDIX A

SLB Interconnections

Trigger Towers 1 to 4

Trigger Towers 5 to 8

ALL SPARE LINES GROUNDED BY A 0 OHM RESISTOR

SYNC1_0 Sync1_1 Sync1_2 Sync1_3 Sync1_4 Sync1_5 Sync1_6 Sync1_7 Sync1_8

SYNC2_0 Sync2_1 Sync2_2 Sync2_3 Sync2_4 Sync2_5 Sync2_6 Sync2_7 Sync2_8

SYNC3_0 Sync3_1 Sync3_2 Sync3_3 Sync3_4 Sync3_5 Sync3_6 Sync3_7 Sync3_8

SYNC4_0 Sync4_1 Sync4_2 Sync4_3 Sync4_4 Sync4_5 Sync4_6 Sync4_7 Sync4_8

GND

GND

GND

GND

SLB - PMC CONNECTORS DESCRIPTION

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Hi Carlos,

Could you clarify a few dimensions on the SLB mechanical drawing? Here is a link to the drawing I am referring to: http://www.physics.umd.edu/hep/HTR/preprod/SLB_SW.pdf

1. Could you give some more details to the locations of the three slb card mounting holes? There is currently only one horizontal dimension of 118 mils.

   ok, I have added more info... let me know if is anything still missing...! see attach

2. Is the vertical location of the 3 PMC connectors centered on the horizontal axis?

   yes...!

3. Is pin 1 of the PMC connectors the longest pin in the upper right hand corner of the connector?

   yes, and this view is the view that is facing the HTR, so the HTR foot print is reversed...!

   the TOP view of the SLB will face the TOP view of the HTR, like a normal PMC board does..!

4. The current horizontal dimensions of the PMC connectors are referenced to the center of pin 1, is it possible to have these dimensions referenced to the center of the connector instead?

   ok... and related to the mech pad, since borders can change...!! depending on the cut...!

cheers

JC
DRAFT - only relative position of the 3 PMC connectors is final
Mapping of Trigger Primitives to differential pairs

Sync1_[8:0] and Sync2_[8:0] → Channel A of the Trigger Link (Vitesse 7216)
Sync3_[8:0] and Sync4_[8:0] → Channel B of the Trigger Link (Vitesse 7216)
Sync5_[8:0] and Sync6_[8:0] → Channel C of the Trigger Link (Vitesse 7216)
Sync7_[8:0] and Sync8_[8:0] → Channel D of the Trigger Link (Vitesse 7216)

Channels A and B are for one \( \eta \) (one tower in width). Channel A transmits \( \Phi_1 \) and \( \Phi_2 \) (each also corresponding to a tower width), with \( \Phi_1 \) transmitted first and \( \Phi_1 < \Phi_2 \). Channel B transmits \( \Phi_3 \) and \( \Phi_4 \), with \( \Phi_3 \) transmitted first and \( \Phi_3 < \Phi_4 \).

Channels C and D are also for one tower-width in \( \eta \). Channels C and D transmit \( \Phi \) in the same order as Channels A and B. If channels A and B are \( \eta_1 \) and channels D and C are \( \eta_2 \), where \(|\eta_1| < |\eta_2|\). [CMS IN 2001/016]

“You may time share the [compression] LUT, using the same LUT for two trigger primitives _IF_ they have the same eta AND they share the same Serial Link Chip Channel (A..D). These two conditions are redundant.” [W. Smith]