

LVDS Output Connections			
DS90CR285 pin	Connection	Notes	
TxIN[0..23]	FPGA I/O		
TxIN[24..27]	GND		
TxOUT0+	J8-2	Route as (+/-) pairs	
TxOUT0-	J8-1	All Traces to J8 equal length within 2mm	
TxOUT1+	J8-4	Traces as short as possible...	
TxOUT1-	J8-3	** SEE DS90CR285 Data Sheet page 15 **	
TxOUT2+	J8-6		
TxOUT2-	J8-5		
TxOUT3+	J8-10		
TxOUT3-	J8-9		
TxCLKOUT+	J8-8		
TxCLKOUT-	J8-7		
LVDS GND	GND		
PLL GND	GND		
PLL VCC	3.3V	One	
LVDS VCC	3.3V		
PWR_DOWN#	3.3V		