

PIN	Row E	Row D	Row C	Row B	Row A
1	L2_D0	GND		GND	L0_D0
2	L2_D1	L2_D2		L0_D2	L0_D1
3	GND	L2_D3		L0_D3	GND
4	L2_D5	L2_D4		L0_D4	L0_D5
5	L2_D6	GND		GND	L0_D6
6	L2_D7	L2_D8		L0_D8	L0_D7
7	GND	L2_D9		L0_D9	GND
8	L2_D11	L2_D10		L0_D10	L0_D11
9	L2_D12	GND		GND	L0_D12
10	L2_D13	L2_D14		L0_D14	L0_D13
11	GND	L2_D15		L0_D15	GND
12					
13		GND		GND	
14					
15	GND				GND
16	L2_D19				
17	L2_CAV*	GND		GND	L0_CAV*
18	L2_DAV*	L2_LNKRDY*		L0_LNKRDY*	L0_DAV*
19	GND	L2_LNKRDY*		L0_LNKRDY*	GND
20	L2_STRBOUT	GND		GND	L0_STRBOUT
21		L2_ERROR		L0_ERROR	
22	GND	L2_ERROR		L0_ERROR	GND
23	GND	GND		GND	GND
24	GND	GND		GND	GND
25	GND	GND		GND	GND
26	L3_CAV*	GND		GND	L1_CAV*
27	L3_DAV*	L3_LNKRDY*		L1_LNKRDY*	L1_DAV*
28	GND	L3_LNKRDY*		L1_LNKRDY*	GND
29	L3_STRBOUT	GND		GND	L1_STRBOUT
30		L3_ERROR		L1_ERROR	
31	GND	L3_ERROR		L1_ERROR	GND
32	L3_D0	GND		GND	L1_D0
33	L3_D1	L3_D2		L1_D2	L1_D1
34	GND	L3_D3		L1_D3	GND
35	L3_D5	L3_D4		L1_D4	L1_D5
36	L3_D6	GND	GND	GND	L1_D6
37	L3_D7	L3_D8	GND	L1_D8	L1_D7
38	GND	L3_D9	GND	L1_D9	GND
39	L3_D11	L3_D10	GND	L1_D10	L1_D11
40	L3_D12	GND	GND	GND	L1_D12
41	L3_D13	L3_D14		L1_D14	L1_D13
42	GND	L3_D15		L1_D15	GND
43					
44		GND		GND	
45			SERIAL		
46	GND		RESET*		GND
47					

Note 1 **L0_xxxxxx** Link 0 signals Keep signals from each link together on schematic
L1_xxxxxx Link 1 signals
L2_xxxxxx Link 2 signals
L3_xxxxxx Link 3 signals

Note 2 There are some duplicated names (I.e. L0_ERROR). Connect both pins together.

Note 3 All Lx_xxxx signals are driven by FPGA through buffers

Note 4 SERIAL driven by FPGA directly (no buffer) with 4.7k pull-up to +3.3V

Note 5 RESET* driven by FPGA through buffer