DFEA2 Reference Manual
S.X.Wu - July 21, 2005

DFEA2 backplane bus timing

DFEA2 requires that BPCLK's rising edge is aligned with the rising edge of the signal NRZC's start bit at the source side (DFEC outputs). Start bit is noted as cycle 0 and a BPCLK cycle contains 7 cycles. DFEA2 samples AS, ADDR, DATA and WRITE signals at the end of cycle 4. Since propagation delay of signals from DFEC compensates themselves to some extent, if DFEC drives backplane signals during cycles 3 through 5, there should be enough setup/hold margin for DFEA2. For read cycles, DFEA2 always asserts the DTACK at the following BPCLK cycle. DFEA2 drives DTACK and DATA lines during cycles 3 through 6, and puts valid data during cycles 4 through 6. If DFEC samples the data at the rising edge of BPCLK, the hold time is guaranteed by the two-way propagation delays, and with three master clock cycles of time, DATA and DTACK setup time should be fine. There are a minimum of three clock cycles for DATA lines' turn-around.

DFEA2 memory map

Address 0  Board CSR
read:
  bit 0    DFEA2 locked to NRZC
  bit 1    DFEA2 detected NRZC lock loss
  bit 2    DFEA2 detected NRZC parity error
  bit 7-3  always '0'
  bit 8    even sector SCL embedded signal mismatch
  bit 9    even sector L1 embedded signal mismatch
  bit 10   even sector SG embedded signal mismatch
  bit 11   even sector FX embedded signal mismatch
  bit 12   odd sector SCL embedded signal mismatch
  bit 13   odd sector L1 embedded signal mismatch
  bit 14   odd sector SG embedded signal mismatch
  bit 15   odd sector FX embedded signal mismatch
write:
  bit 0    reset
Address 1  Control bits delay
Bits 7-3 determine how many events to delay.
Bits 2-0 determine the relative position of global EOF signal and link EOFs)

read:
  bit 7-0         delay value
  bit 15-8        always '0'

write:
  bit 7-0         delay value
  bit 15-8        not used

Address 2  Fake and capture control register

read:
  bit 15-6        read as '0'
  bit 5-4         if set, will return to '0' after command executed
  bit 3-2         read as '0'
  bit 1-0         as written

write:
  bit 15-10       not used
  bit 9           capture input and L1 out once
  bit 8           inject and capture corresponding input and L1/L2 out once
  bit 7-6         not used
  bit 5           capture corresponding input and L1/L2 output when receiving next L1
  bit 4           inject fake data when receiving next FX
  bit 3-2         not used
  bit 1           inject at every FX
  bit 0           inject as long as it is '1'

Address 3  FPGA CSR

read:
  bit 0           FPGA U7 done signal
bit 1  FPGA U8 done signal  
bit 2  U9 FPGA done signal  
bit 3  U10 FPGA done signal  
bit 4  U7 FPGA init signal when bit 0 = '0',  
       otherwise U7 FPGA DCM lock signal  
bit 5  U8 FPGA init signal when bit 1 = '0',  
       otherwise U7 FPGA DCM lock signal  
bit 6  U9 FPGA init signal when bit 2 = '0',  
       otherwise U7 FPGA DCM lock signal  
bit 7  U10 FPGA init signal when bit 3 = '0',  
       otherwise U7 FPGA DCM lock signal  
bit 15-8 DFEA2 board serial number

write:

bit 0  U7 FPGA reprogram start  
bit 1  U8 FPGA reprogram start  
bit 2  U9 FPGA reprogram start  
bit 3  U10 FPGA reprogram start  
bit 11-4 not used  
bit 12  U7 FPGA DCM reset  
bit 13  U8 FPGA DCM reset  
bit 14  U9 FPGA DCM reset  
bit 15  U10 FPGA DCM reset

**Address 4  U7 FPGA program data register**

read:

bit 15-0  U7 firmware revision number  
          (7 as of 7/8/2005)

write:

bit 7-0  first byte of configuration data  
bit 15-8 second byte of configuration data

**Address 5  U8 FPGA program data register**

read:

bit 15-0  U8 firmware revision number  
          (8 as of 7/8/2005)
write:
  bit 7-0    first byte of configuration data
  bit 15-8   second byte of configuration data

**Address 6**  U9 FPGA program data register
read:
  bit 15-0   U8 firmware revision number
              (7 as of 7/8/2005)
write:
  bit 7-0    first byte of configuration data
  bit 15-8   second byte of configuration data

**Address 7**  U10 FPGA program data register
read:
  bit 15-0   U10 firmware revision number
              (8 as of 7/8/2005)
write:
  bit 7-0    first byte of configuration data
  bit 15-8   second byte of configuration data

**Address 8**  History register A (read-only)
  bit 0       even sector tick_turn_locked
  bit 1       even sector valid_trk
  bit 2       even sector SG_err
  bit 3       even sector bad FX
  bit 4       odd sector tick_turn_locked
  bit 5       odd sector valid_trk
  bit 6       odd sector SG_err
  bit 7       odd sector bad FX
  bit 8       SCL seen
  bit 9       L1 seen
  bit 10      SG seen
  bit 11      FX seen
  bit 15-12   always '0'

**Address 9**  History register B (read-only)
bit 7-0          corresponding link clock frequency error  
nbit 15-8        corresponding link sync error

Address 0xa: History register c (read-only)
  bit 7-0 corresponding link period error
  bit 15-8 corresponding link pattern error

Address 0xb: L2 pipeline depth register.
(Due to code change, the new depth value should be three less than the original value)
write
  bit 6-0 L2 pipeline depth register
  bit 15-7 not used

read
  bit 6-0 even channel L2 pipeline depth readback
  bit 7       always '0'
  bit 14-8   odd channel L2 pipeline depth readback
  bit 15      always '0'

Address 0xc: U6(backplane control)firmware version
  (0xc as of 7/8/2005)

Address 0xd: Tick number register (read-only)
  bit 15-0 tick number of injected event when writing 0x100 to address 2

Address 0xe: Turn number register (read-only)
  bit 7-0 turn number of injected event when writing 0x100 to address 2
  bit 9-8 lvds_in of injected event
  bit 11-10 lvds_out of injected event
  bit 12      FX bit of injected event
  bit 13      SCL bit of injected event
  bit 14      not used
  bit 15      L1 rule violation flag of injected event(L1 spacing less than 6 ticks) If set, do not check captured L2CFT and L2CPS
**Address 0xf: Display register for access test**

This register has two functions. First is to provide a Read/write register for testing backplane access.

Secondly, its bit 11-8 multiplex signals to be seen at the front panel test points:

when bits 11-8 = "0001"

- position 1: ground
- position 2: U6 NRZC data signal
- position 3: U6 NRZC start bit
- position 4: U6 NRZC locked
- position 5: U7 EOF at the FPGA pad input
- position 6: ground
- position 7: ground
- position 8: LVDS link1 sync monitor. It is an overlap of the link side frame bit and global side clear signal delayed by two clock cycles. Changing the three LSBs of NRZC delay value to make the delayed clear signal following the frame bit as close as possible but do not overlap.
  - position 9: even sector L1_embedded
  - position 10: even sector L1
  - position 11: even sector FX_embedded
  - position 12: even sector FX
  - position 13: odd sector L1_embedded
  - position 14: odd sector L1
  - position 15: odd sector FX_embedded
  - position 16: odd sector FX
  - position 17: U9 EOF at the FPGA pad input
  - position 18: ground
  - position 19: ground
  - position 20: same as position 8, but for LVDS link5

when bits 11-8 = "0010"

- position 1: ground
- position 2: ground
- position 3: ground
- position 4: ground
position 5: U7 EOF at the FPGA pad input
position 6: ground
position 7: ground
position 8: LVDS link2 sync monitor.
position 9: even sector SG_embedded
position 10: even sector SG
position 11: even sector SCL_embedded
position 12: even sector SCL
position 13: odd sector SG_embedded
position 14: odd sector SG
position 15: odd sector SCL_embedded
position 16: odd sector SCL
position 17: U9 EOF at the FPGA pad input
position 18: ground
position 19: ground
position 20: same as position 8, but for LVDS link6

when bits 11-8 = "0011"
position 1: ground
position 2: ground
position 3: ground
position 4: ground
position 5: U7 EOF at the FPGA pad input
position 6: LVDS link2 bit 3 delayed by two link2_clk cycles
position 7: LVDS link2 bit 1 delayed by two link2_clk cycles
position 8: LVDS link3 sync monitor.
position 9: even sector muon_pe
position 10: even sector muon_dat(15)
position 11: even sector L1 header with FX bit set
position 12: even sector L2CFT header
position 13: odd sector muon_pe
position 14: odd sector muon_dat(15)
position 15: odd sector L1 header with FX bit set
position 16: odd sector L2CFT header
    Note: signals from pos 9 thru 16 are two clock cycles later than the actual signals at the FPGA pad outputs.
position 17: U9 EOF at the FPGA pad input
position 18: LVDS link7 bit 3 delayed by two link7_clk cycles
position 19: LVDS link7 bit 1 delayed by two link7_clk cycles
position 20: LVDS link7 sync monitor.

when bits 11-8 = "0100"
position 1: ground
position 2: ground
position 3: ground
position 4: ground
position 5: U7 EOF at the FPGA pad input
position 6: ground
position 7: ground
position 8: LVDS link4 sync monitor.
position 9: U8 EOF at the FPGA pad input
position 10: U8 DCM_LOCK
position 11: ground
position 12: ground
position 13: U10 EOF at the FPGA pad input
position 14: U10 DCM_LOCK
position 15: ground
position 16: ground
position 17: U9 EOF at the FPGA pad input
position 18: ground
position 19: ground
position 20: LVDS link8 sync monitor.

when bits 11-8 = "0101": All position should have pulsing output. This is for assembly integrity test only.

when bits 11-8 = "1111":
position 4: U6 clock
position 5: U7 clock
position 9: U8 clock
position 13: U10 clock
position 17: U9 clock
other positions: ground
when others : all test point outputs ground level.
   To reduce system noise, this register
   should be all ‘0’ during data taking.

**Address 0x10-16: Even sector muon data capture(read-only)**

**Address 0x18-1e: odd sector muon data capture(read-only)**

Note: for data word longer than 16 bits, lower 16 bits always in even addresses

**Address 0x20-2d: even sector L1 data capture(read-only)**

**Address 0x30-3d: odd sector L1 data capture(read-only)**

**Address 0x40-55: even sector L2CPS data capture(read-only)**

**Address 0x60-75: odd sector L2CPS data capture(read-only)**

**Address 0x80-B5: even sector L2CFT data capture(read-only)**

**Address 0xB8: even sector sector register**
   - bit 6-0 sector
   - bit 15-7 for test only

**Address 0xB9: even sector bus register**
   - bit 0  muon_patt
   - bit 1  muon_fake
   - bit 2  ctoc_zero
   - bit 3  ctoc_patt
   - bit 5-4 ctoc_fake_sel
   - bit 7-6 ctoc_L2_fake
   - bit 15-8 not used

**Address 0xC0-F5: odd sector L2CFT data capture(read-only)**

**Address 0xF8: odd sector sector register**
bit 6-0 sector
bit 15-7 for test only

**Address 0xF9: odd sector bus register**

- bit 0 muon_patt
- bit 1 muon_fake
- bit 2 ctoc_zero
- bit 3 ctoc_patt
- bit 5-4 ctoc_fake_sel
- bit 7-6 ctoc_L2_fake
- bit 15-8 not used

**Address 0x100-10D: link1 data capture(read-only)**

**Address 0x110-11D: link2 data capture(read-only)**

**Address 0x120-12D: link3 data capture(read-only)**

**Address 0x130-13D: link4 data capture(read-only)**

**Address 0x140-14D: link5 data capture(read-only)**

**Address 0x150-15D: link6 data capture(read-only)**

**Address 0x160-16D: link7 data capture(read-only)**

**Address 0x170-17D: link8 data capture(read-only)**

**Address 0x180-18D: link1 fake data**

**Address 0x190-19D: link2 fake data**

**Address 0xA0-1AD: link3 fake data**

**Address 0xB0-1BD: link4 fake data**
Address 0x1C0-1CD: link5 fake data

Address 0x1D0-1DD: link6 fake data

Address 0x1E0-1ED: link7 fake data

Address 0x1F0-1FD: link8 fake data

LED display

red LED on the left: 3.3V
red LED on the right: 1.5V
top green LED on the left: all FPGAs’ DONE high
top green LED on the right: DTACK

The rest of eight green LEDs display a page of one byte information:
left column has odd bits with MSB bit 7 on the top.
right column has even bit with LSB bit0 at the bottom.

Page 0        (power on default): bit 7-4 displays INIT signals of U10-U7
               if corresponding done is '0'
               or DCM lock when '1'
               bit 3-0 display DONE signals of U10-U7

Page 1 : link clock error for LVDS channels 8-1

Page 2 : link sync error for LVDS channels 8-1

Page 3 : link period error for LVDS channels 8-1

Page 4 : link pattern error for LVDS channels 8-1

Page 5 :
bit 7   embedded mismatch in LVDS 5-8
       bit 6   embedded mismatch in LVDS 1-4
       bit 5   FX signal received
       bit 4   SG signal received
       bit 3   L1 signal received
bit 2  SCL signal received
bit 1  NRZC start bit locked
bit 0  NRZC parity error

Page 6 : DFEA2 Serial Number

Page 7 : lower byte of display register

**Front Panel TEST points**

The 40-pin front panel header provides access of test signals from the FPGAs

The right column pins are all grounds.
The left column are signals
The positions are counted from top through bottom as 1 thru 20.
Refer to display register 0xf for details

LVDS link inputs:
link1  red cable from sector N-1
link2  brown cable from sector N
link3  green cable from sector N
link4  purple cable from sector N
link5  red cable from sector N+1
link6  yellow cable from sector N+1
link7  blue cable from sector N+1
link8  green cable from sector N+2

**JTAG chain order:**

U10, U8, U6, U22, U7 and U9

**FPGA programming procedure:**

1. write to address 0x3 to start reprogramming
2. read from address 0x3 and wait until init is high
3. write configuration data to FPGA program data register, two byte at a time, lower byte will be sent out first.
4. read from address 0x3 and check done goes high
5. write to address 0x3 to reset DCM
6. read from address 0x3 and check init is high