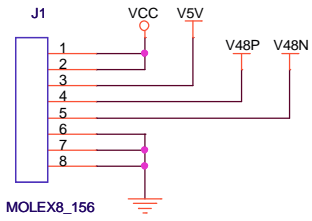


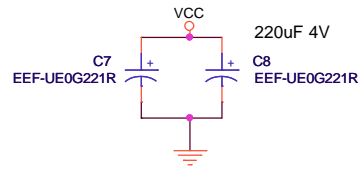
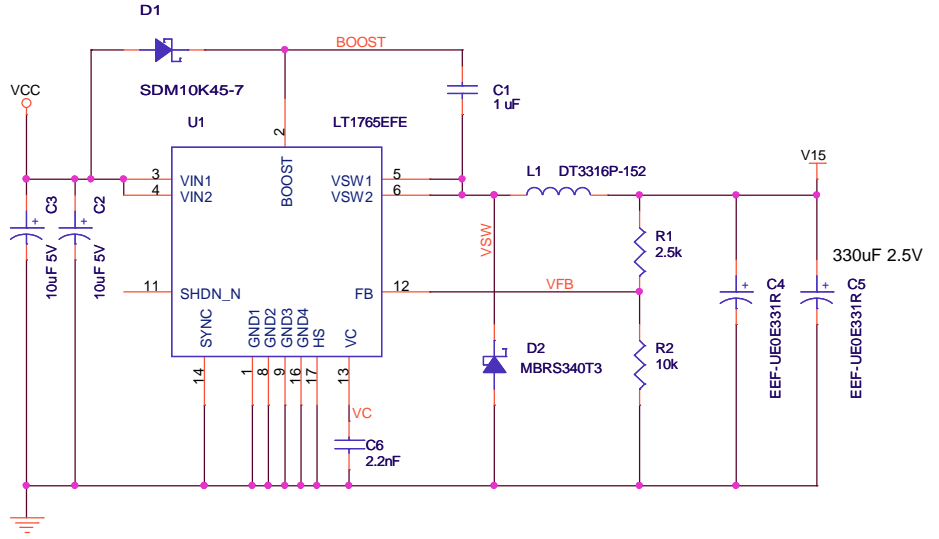
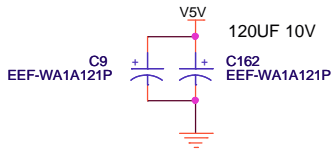
Title		
DSAT Tester Schematic		
Size	Document Number	Rev
Custom	<Doc>	A
Date:	Tuesday, June 08, 2004	Sheet 1 of 24

1.5V FPGA core power regulator



LEGEND

- 1 - 3.3V
- 2 - 3.3V
- 3 - 5V
- 4 - +48V
- 5 - -48V
- 6 - GND
- 7 - GND
- 8 - GND

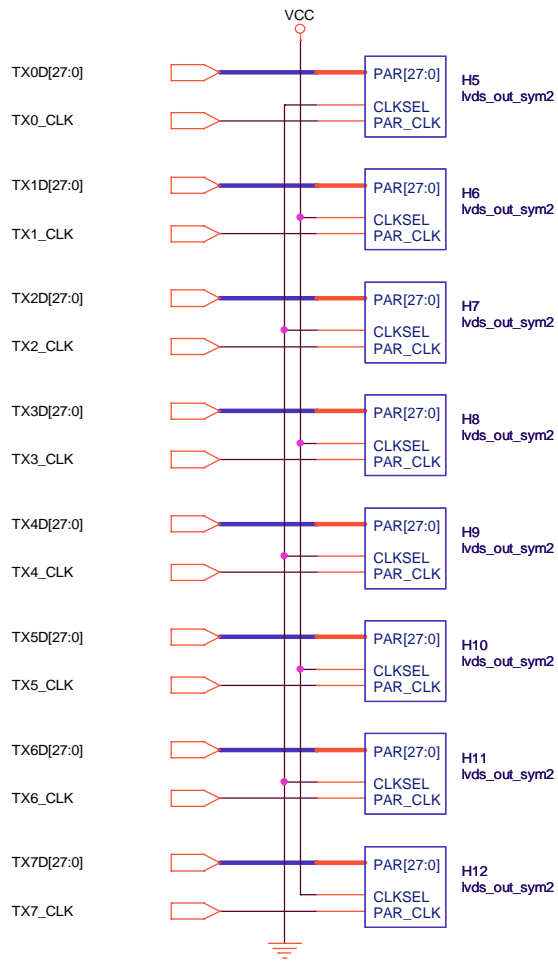


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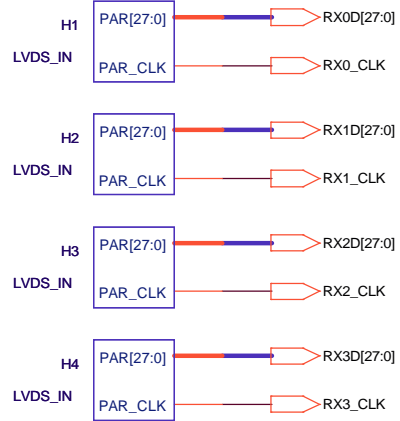
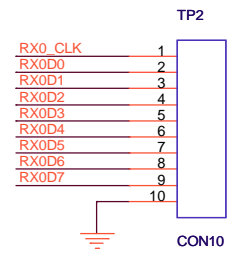
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D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	Power Input	A
Date:	Thursday, June 10, 2004	Sheet 2 of 24



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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
	Bypass Capacitors	A
Date:	Tuesday, June 08, 2004	Sheet 3 of 24

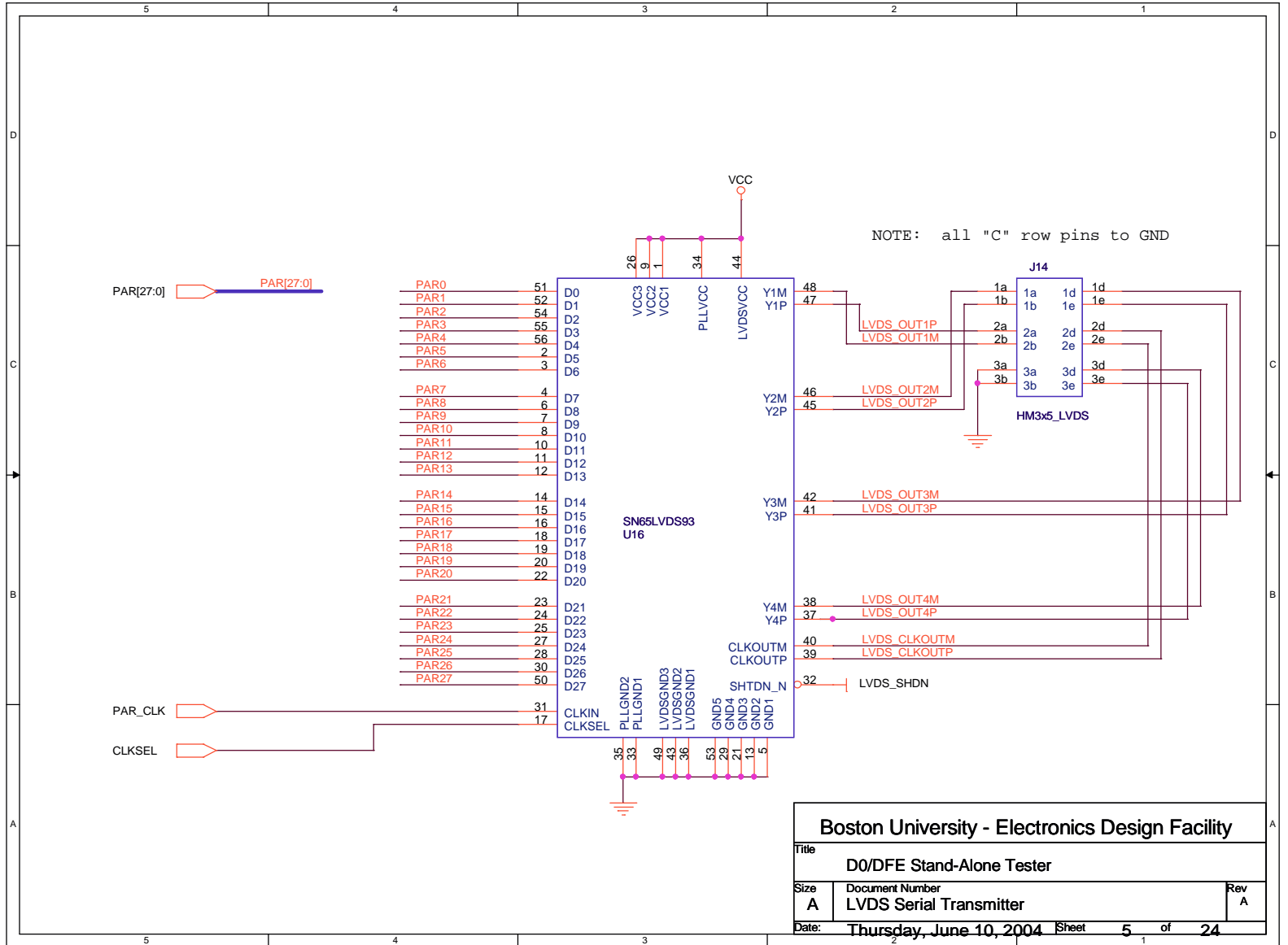


LEGEND
 1 - RX0_CLK
 2-9 - RX0[7:0]
 10 - GND

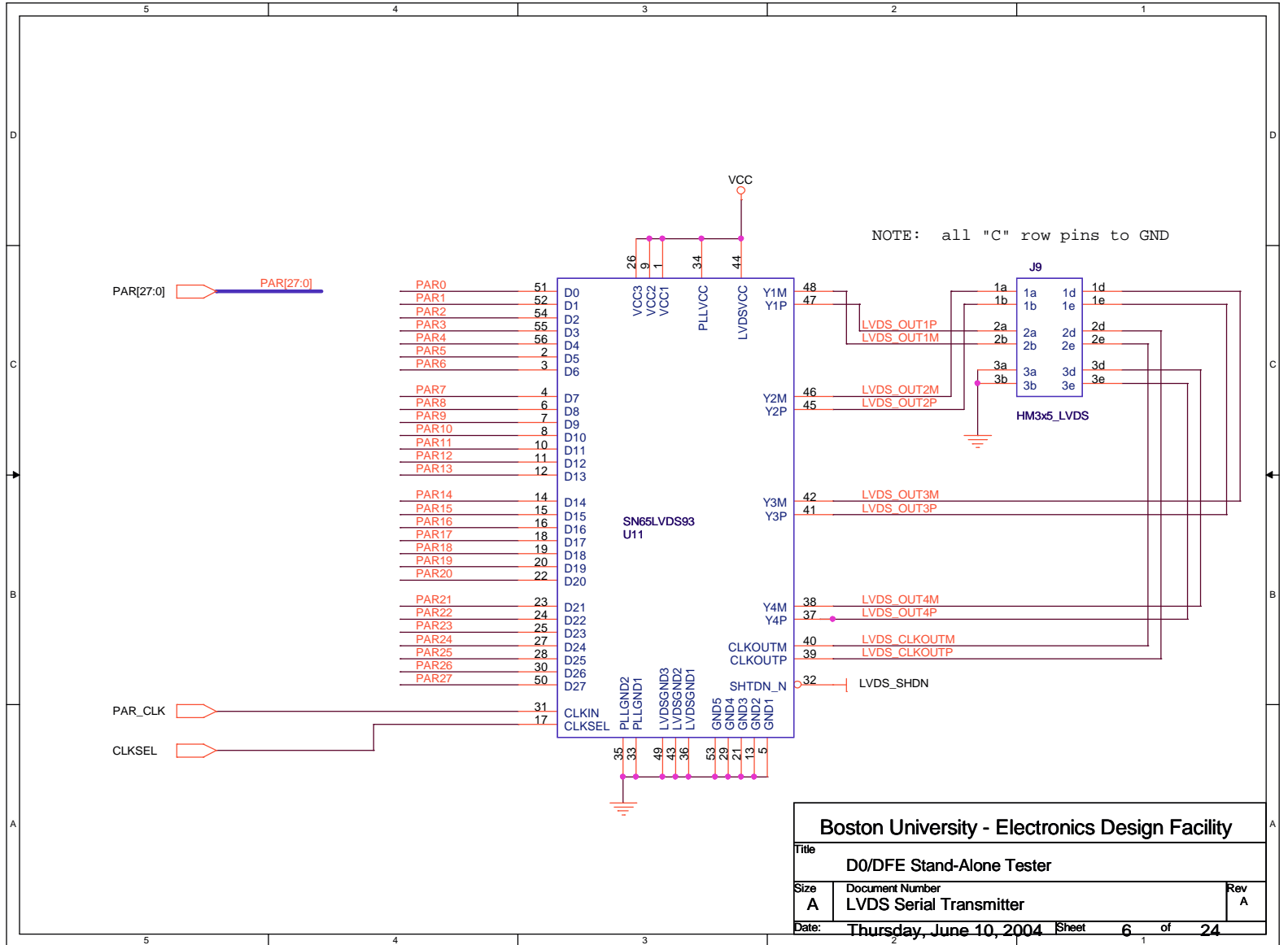


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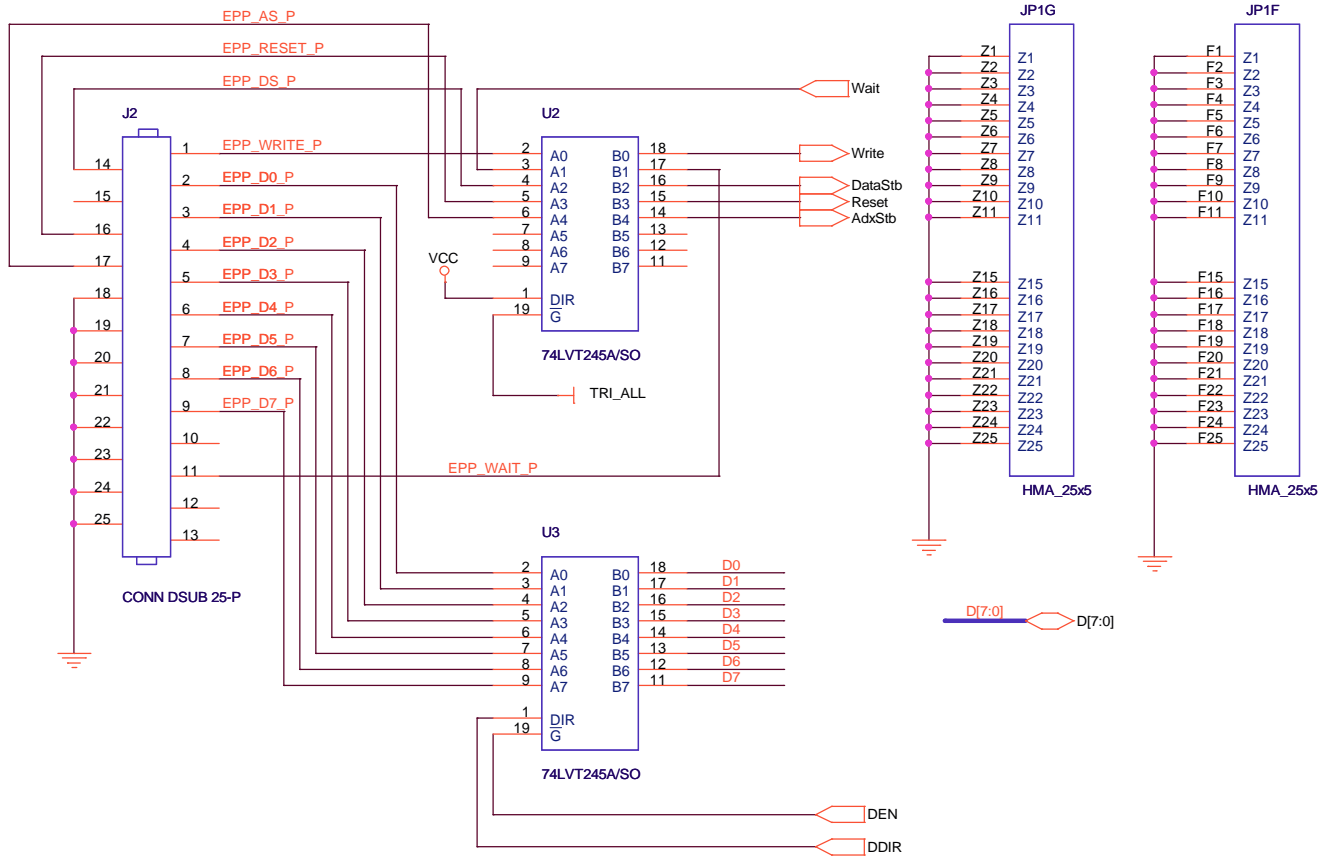
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D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial I/O	A
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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Thursday, June 10, 2004	Sheet 5 of 24

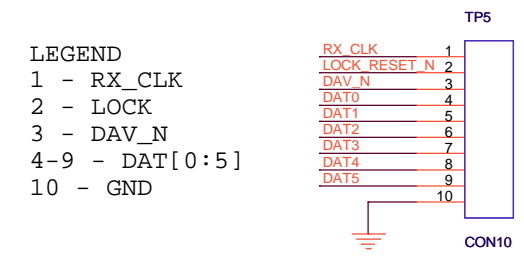
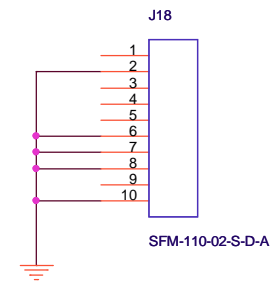
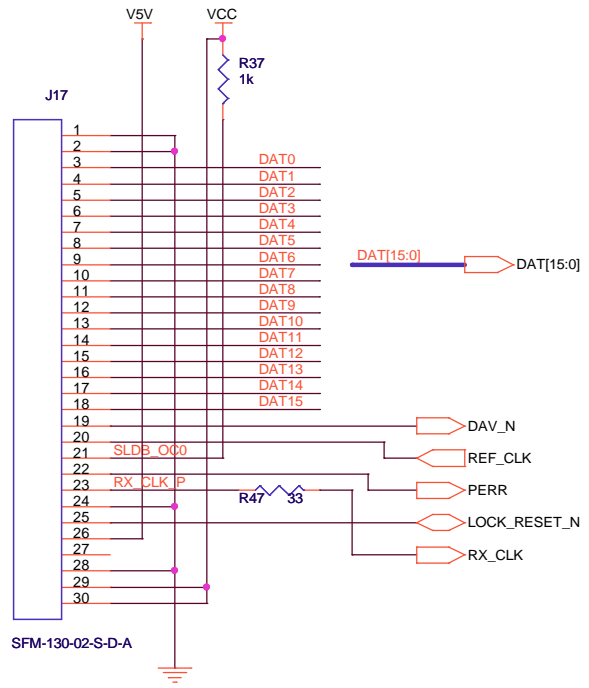


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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Thursday, June 10, 2004	Sheet 6 of 24



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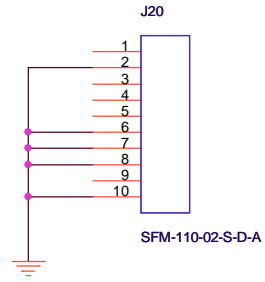
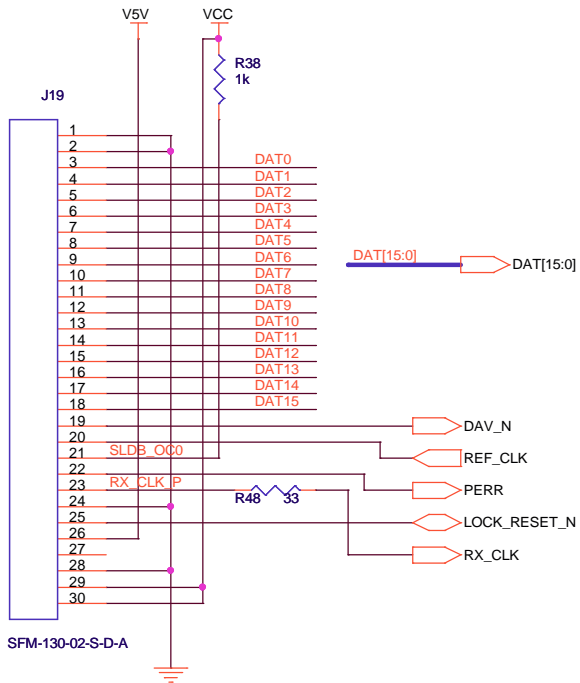
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D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	EPP Parallel Port	A
Date:	Thursday, June 10, 2004	Sheet 7 of 24



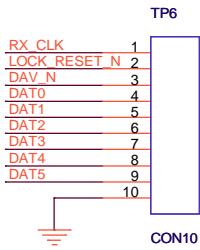
LEGEND
 1 - RX_CLK
 2 - LOCK
 3 - DAV_N
 4-9 - DAT[0:5]
 10 - GND

SLDB Serial Link Receiver
 See spec sheet for connector placement

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Title D0/DFE Stand-Alone Tester		
Size A	Document Number SLDB Serial Link Receiver	Rev A
Date: Tuesday, June 08, 2004 Sheet 8 of 24		

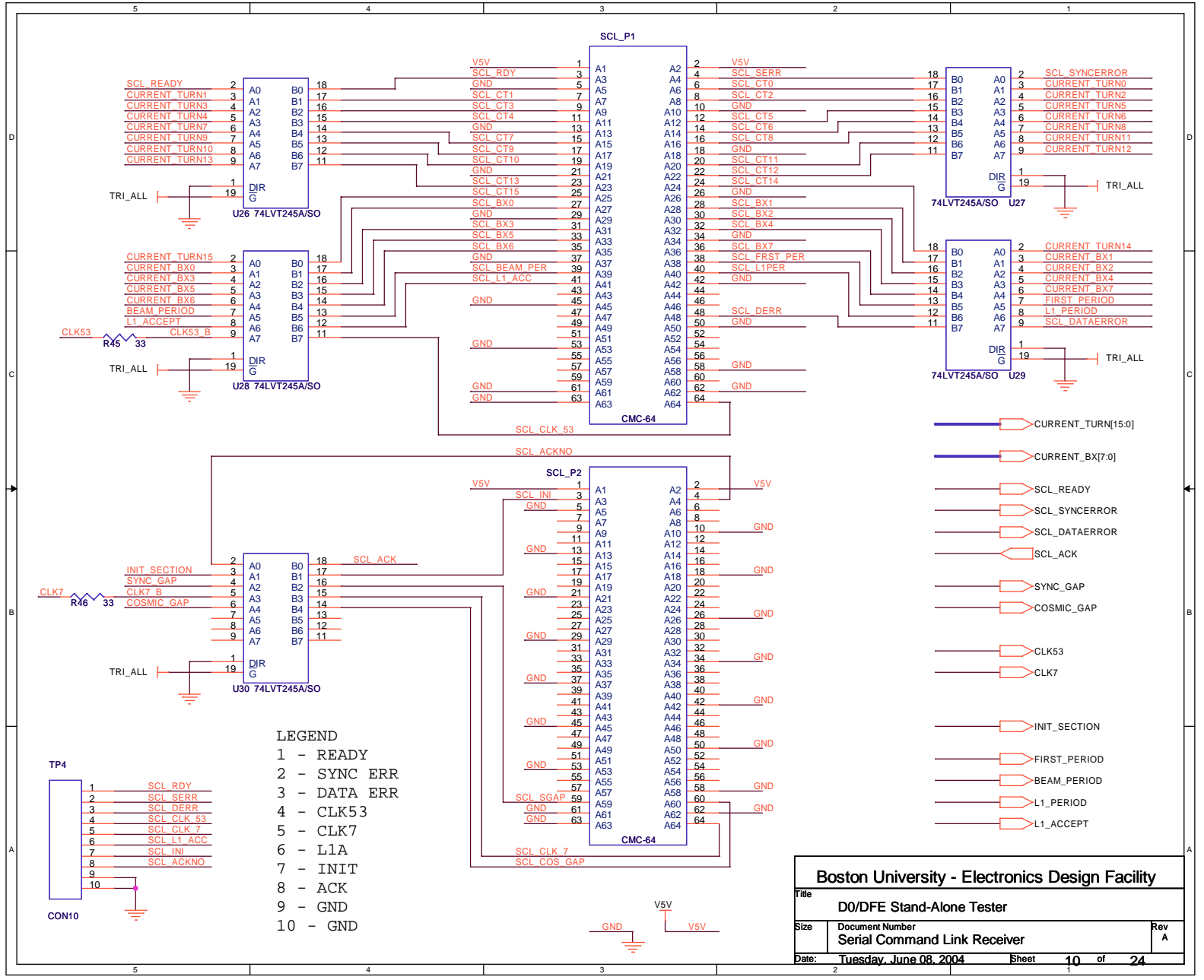


LEGEND
 1 - RX_CLK
 2 - LOCK
 3 - DAV_N
 4-9 - DAT[0:5]
 10 - GND



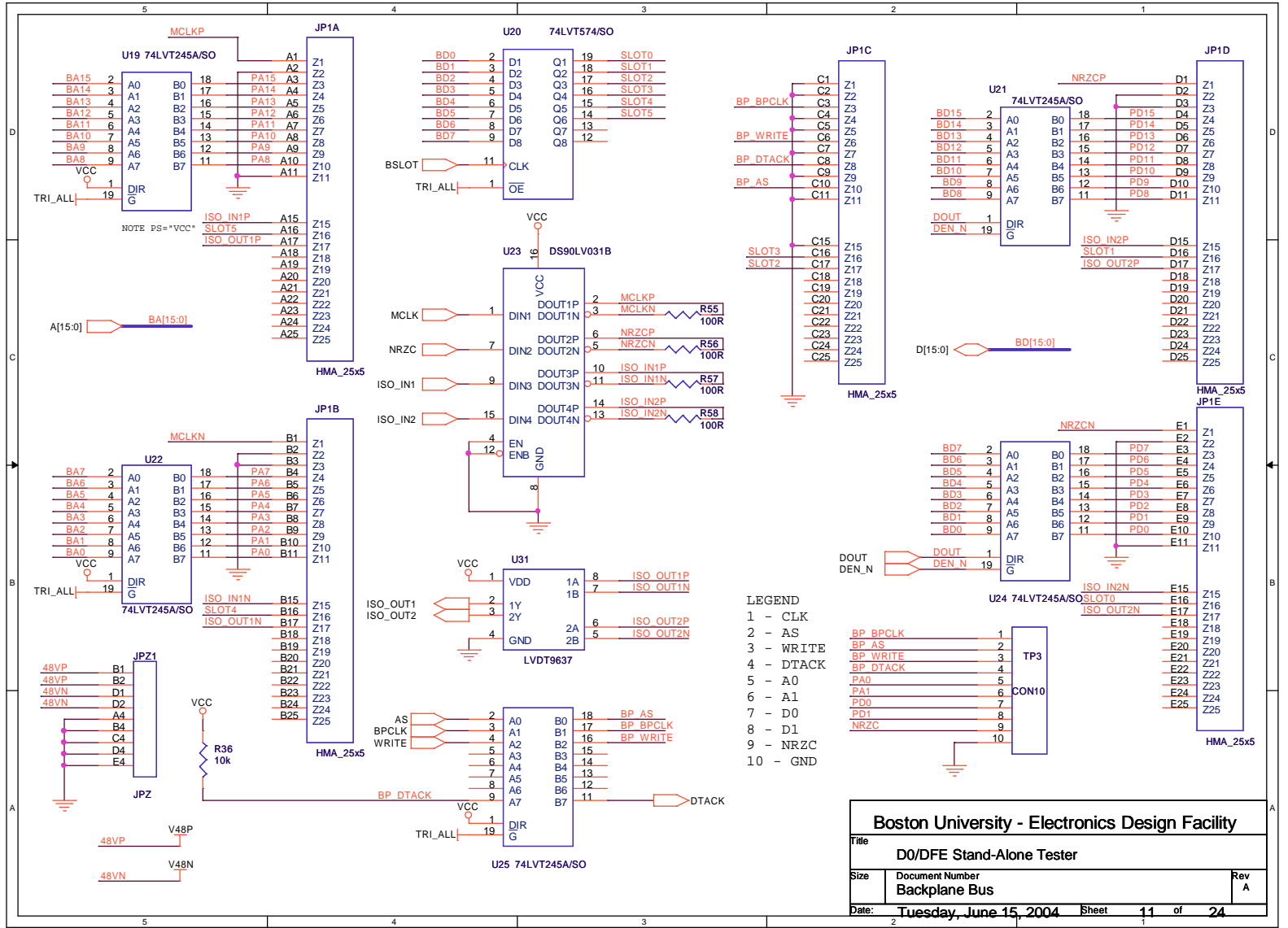
SLDB Serial Link Receiver
 See spec sheet for connector placement

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number SLDB Serial Link Receiver	Rev A
Date: Tuesday, June 08, 2004 Sheet 9 of 24		

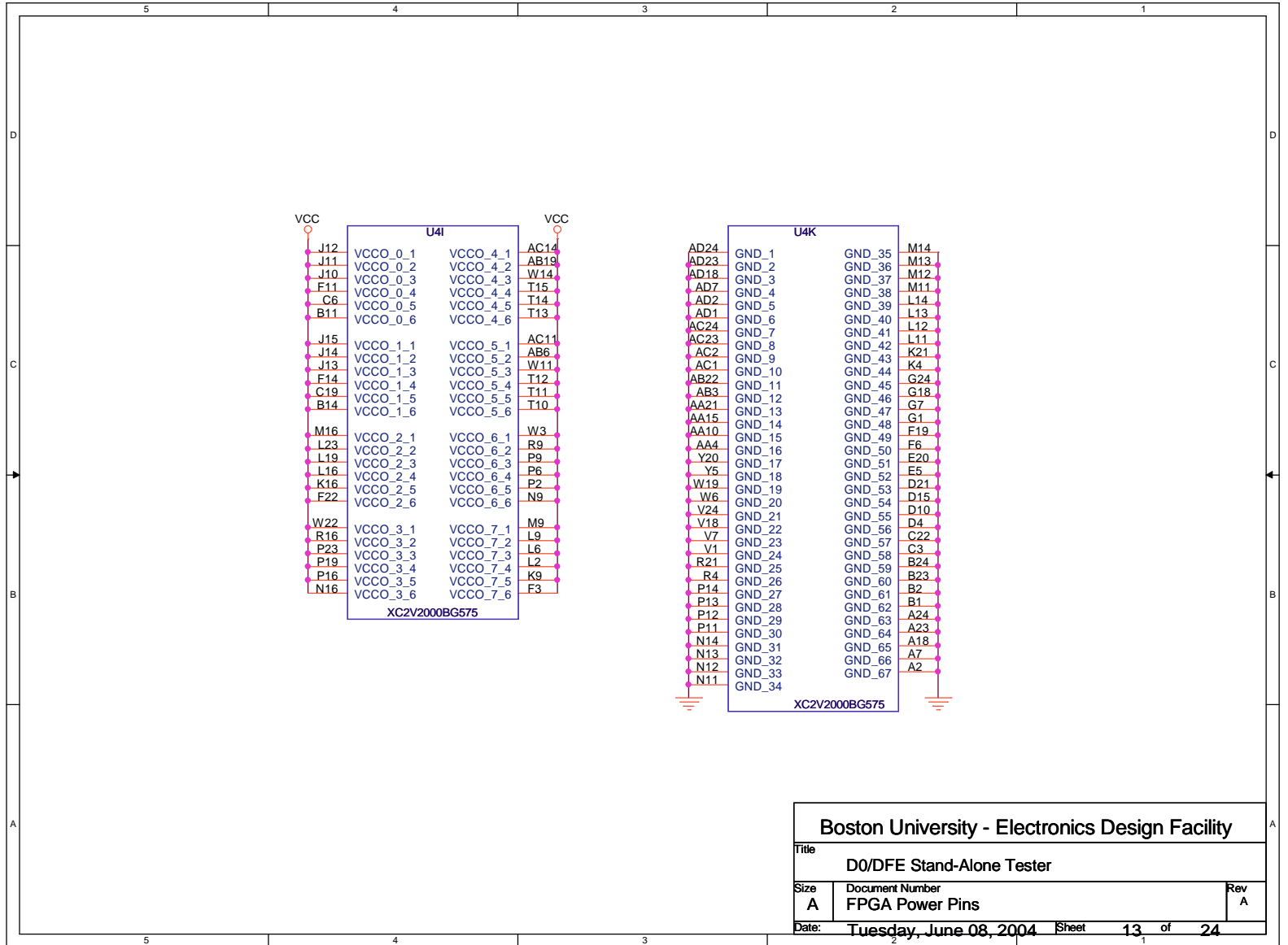


- LEGEND**
- 1 - READY
 - 2 - SYNC ERR
 - 3 - DATA ERR
 - 4 - CLK53
 - 5 - CLK7
 - 6 - L1A
 - 7 - INIT
 - 8 - ACK
 - 9 - GND
 - 10 - GND

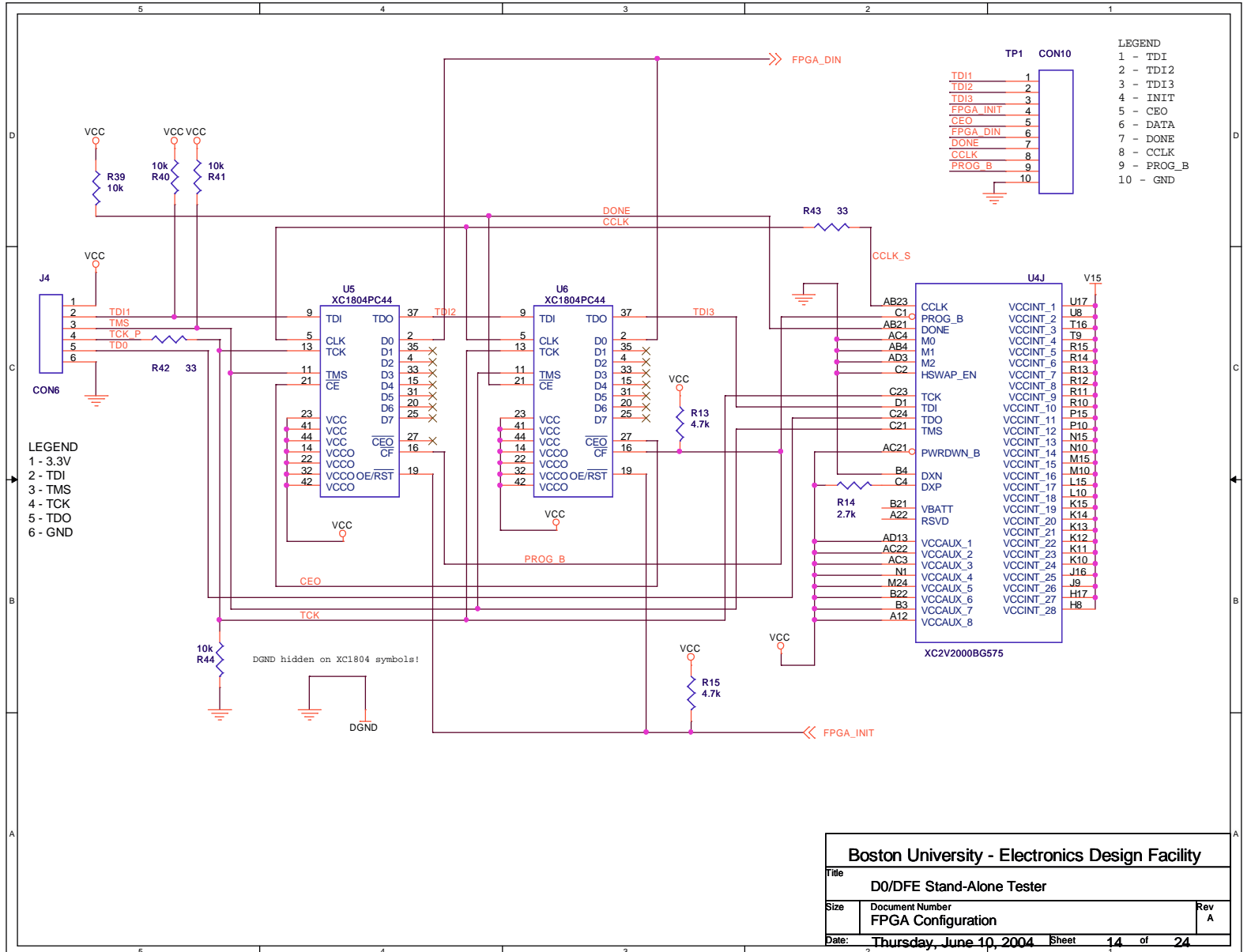
Boston University - Electronics Design Facility		
Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
	Serial Command Link Receiver	A
Date:	Tuesday, June 08, 2004	Sheet 10 of 24

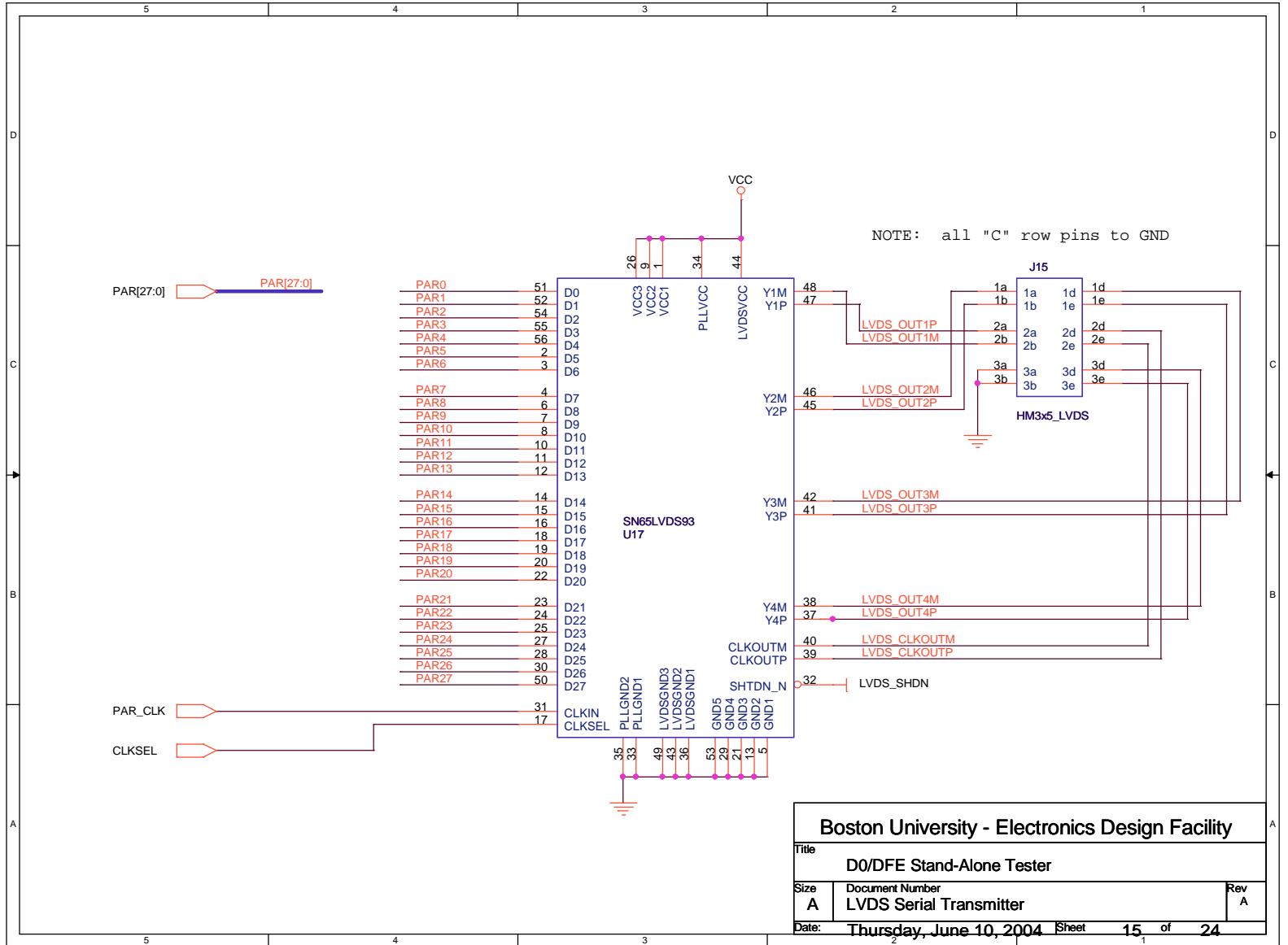


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Title		
D0/DFE Stand-Alone Tester Backplane Bus		
Size	Document Number	Rev
		A
Date:	Tuesday, June 15, 2004	Sheet 11 of 24

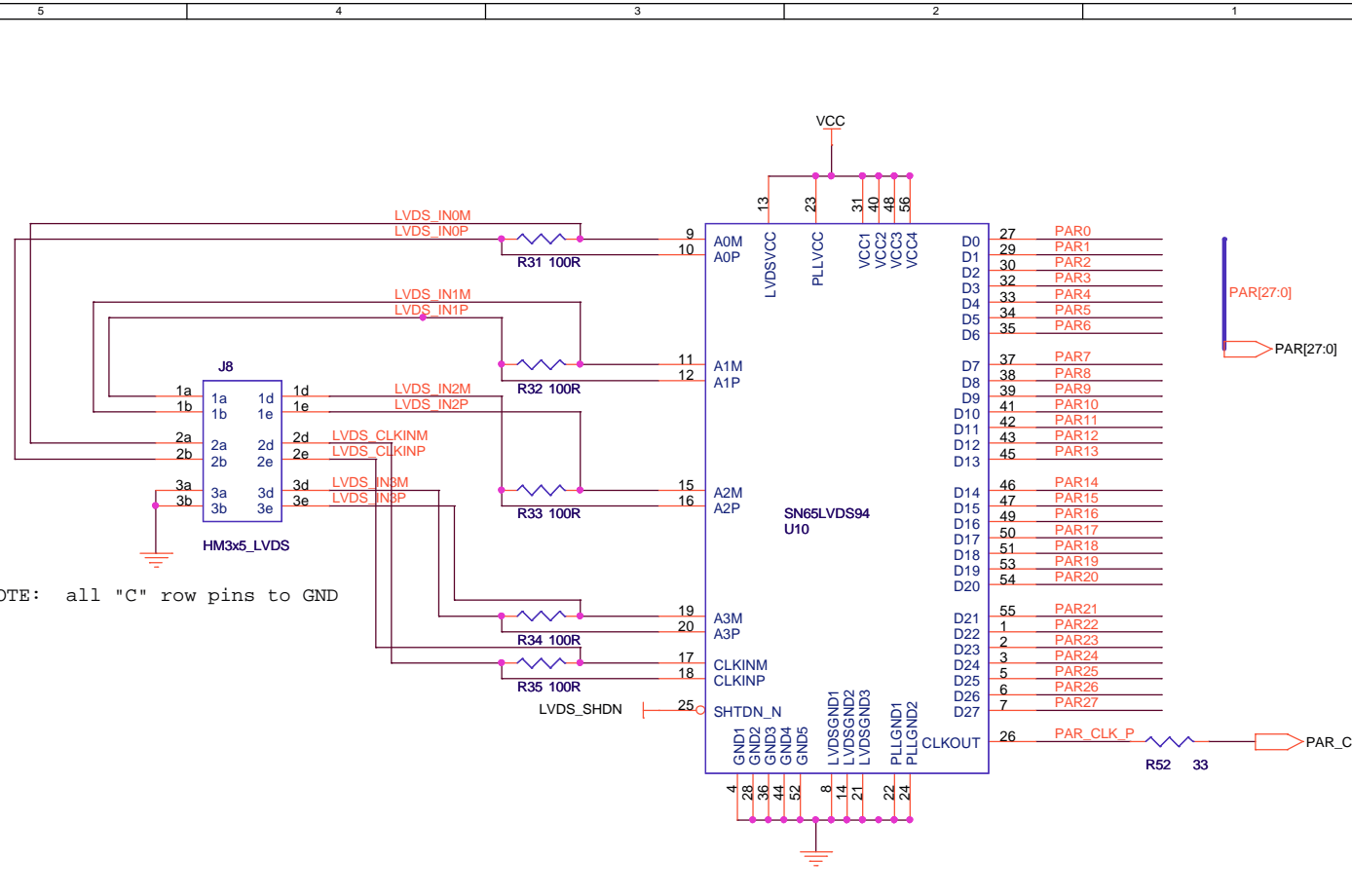


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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	FPGA Power Pins	A
Date:	Tuesday, June 08, 2004	Sheet 13 of 24



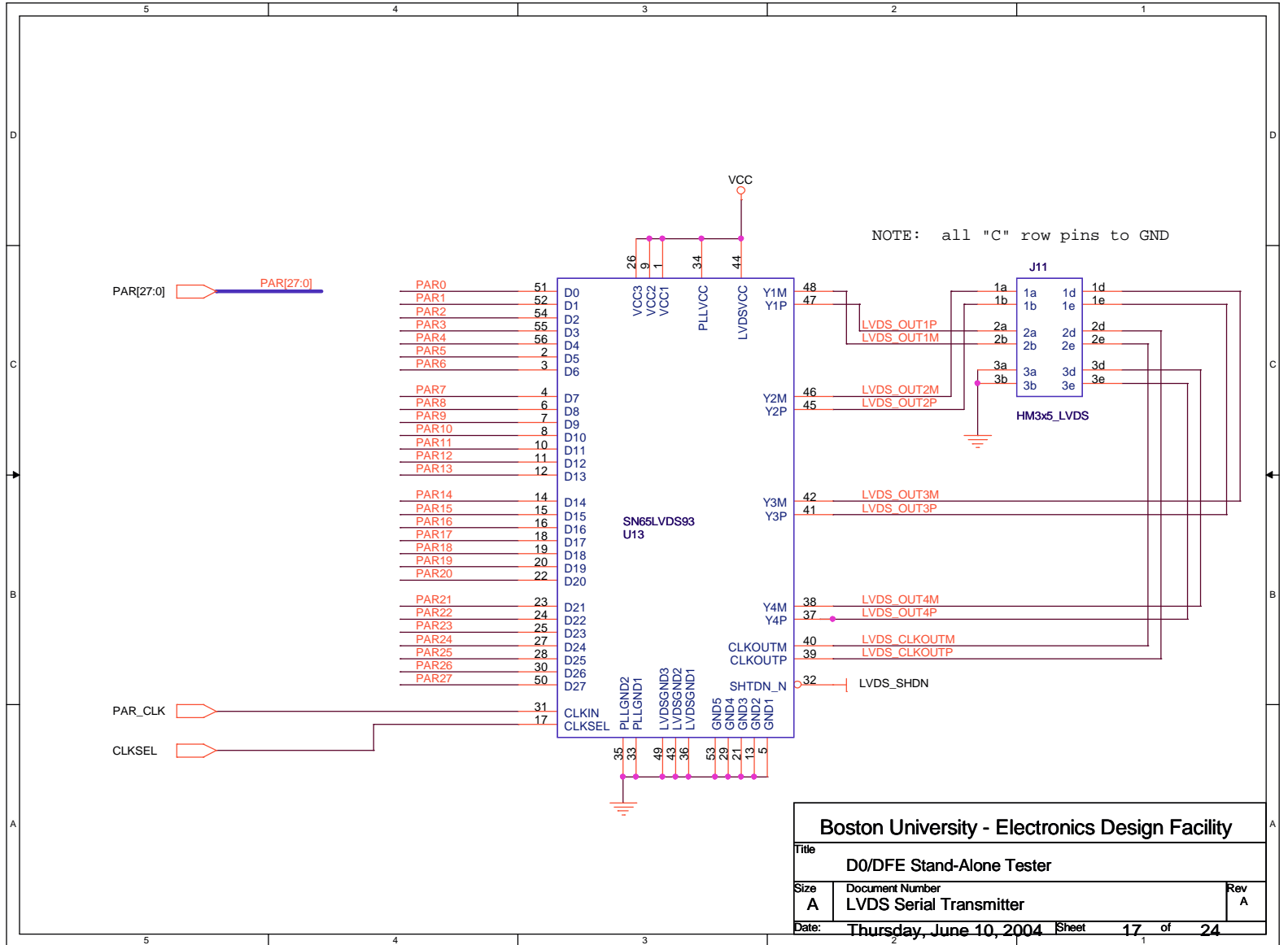


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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Thursday, June 10, 2004	Sheet 15 of 24

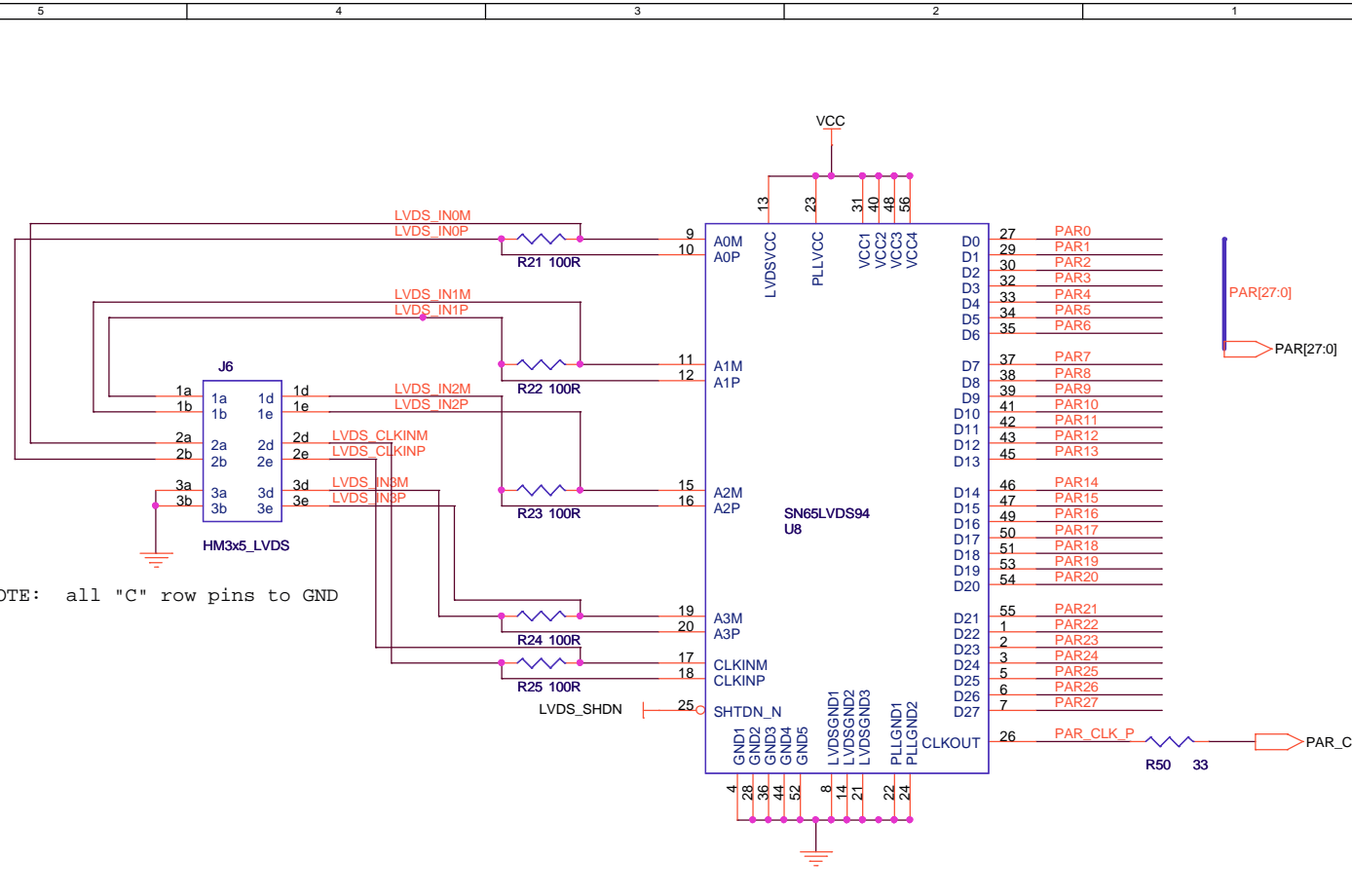


NOTE: all "C" row pins to GND

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Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Receiver	Rev A
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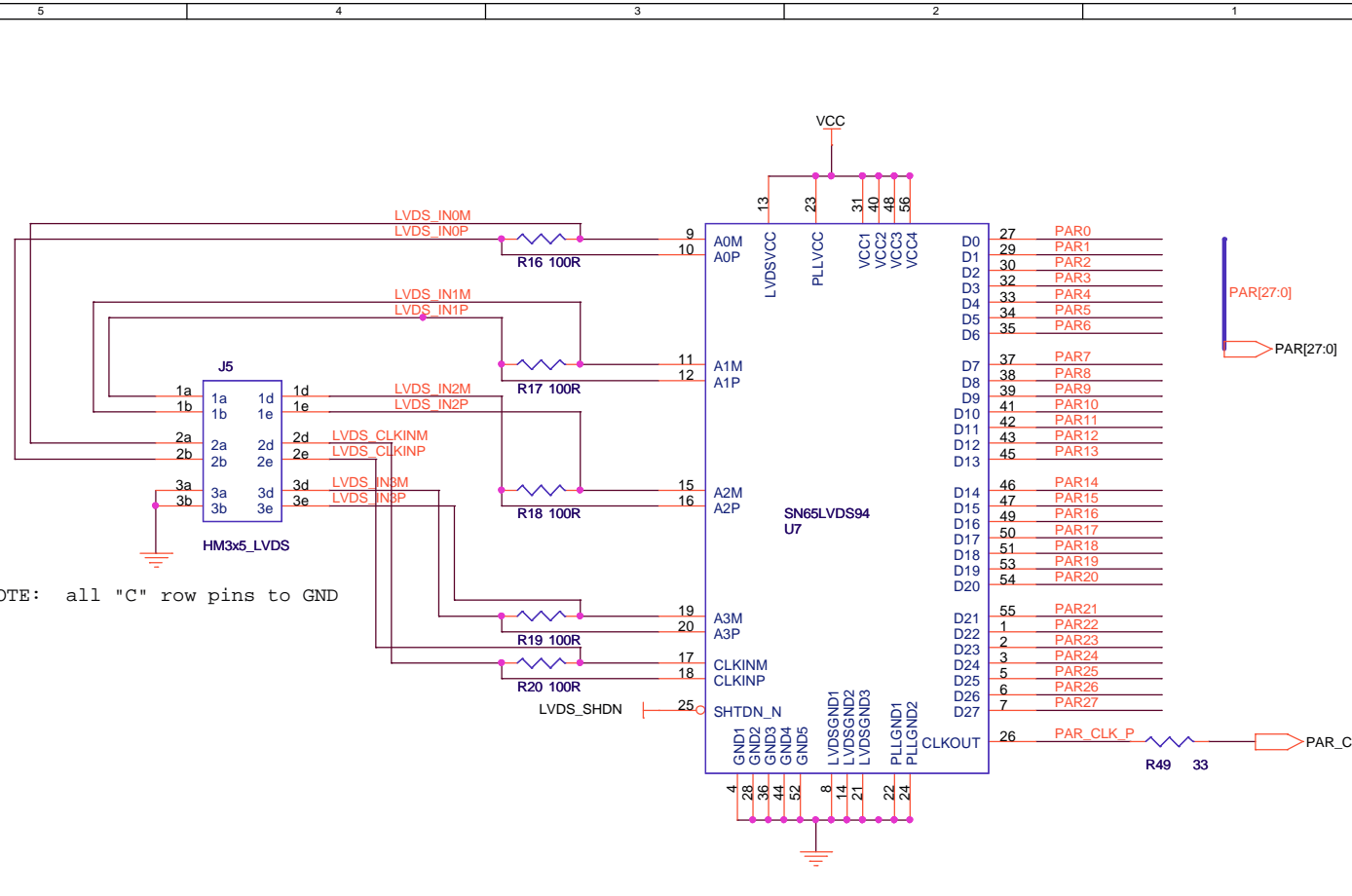


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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Thursday, June 10, 2004	Sheet 17 of 24



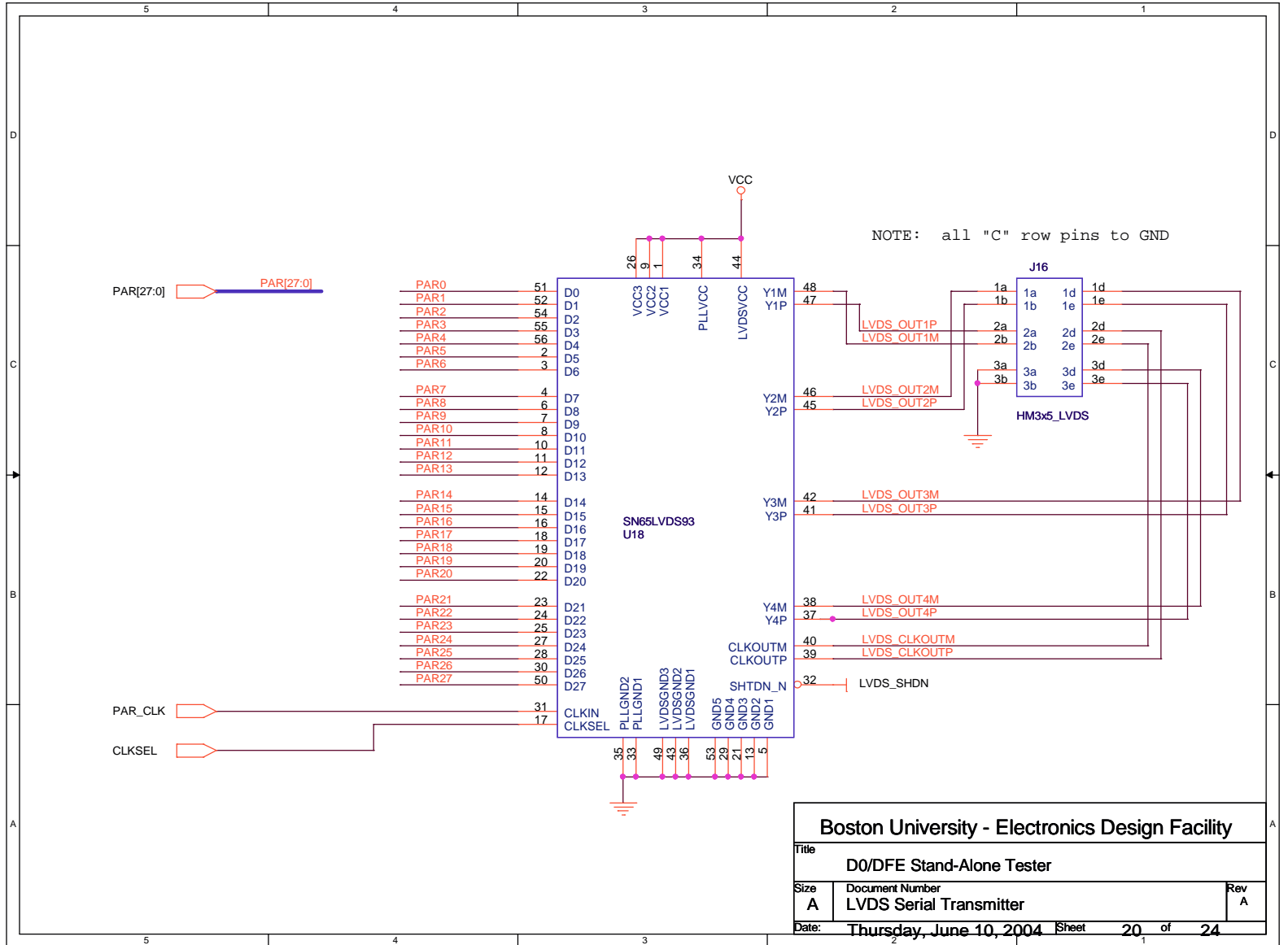
NOTE: all "C" row pins to GND

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Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Receiver	Rev A
Date: Thursday, June 10, 2004 Sheet 18 of 24		

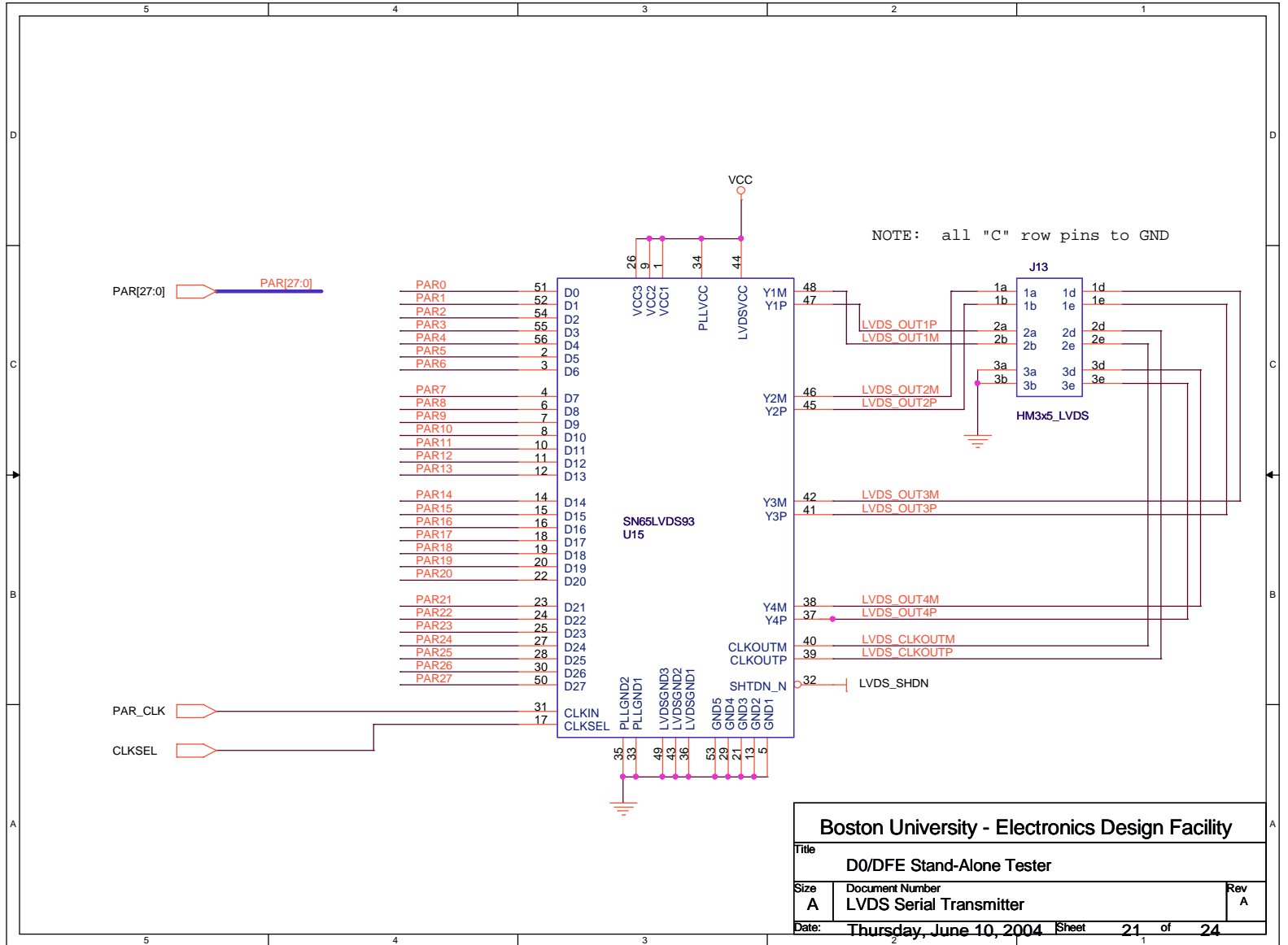


NOTE: all "C" row pins to GND

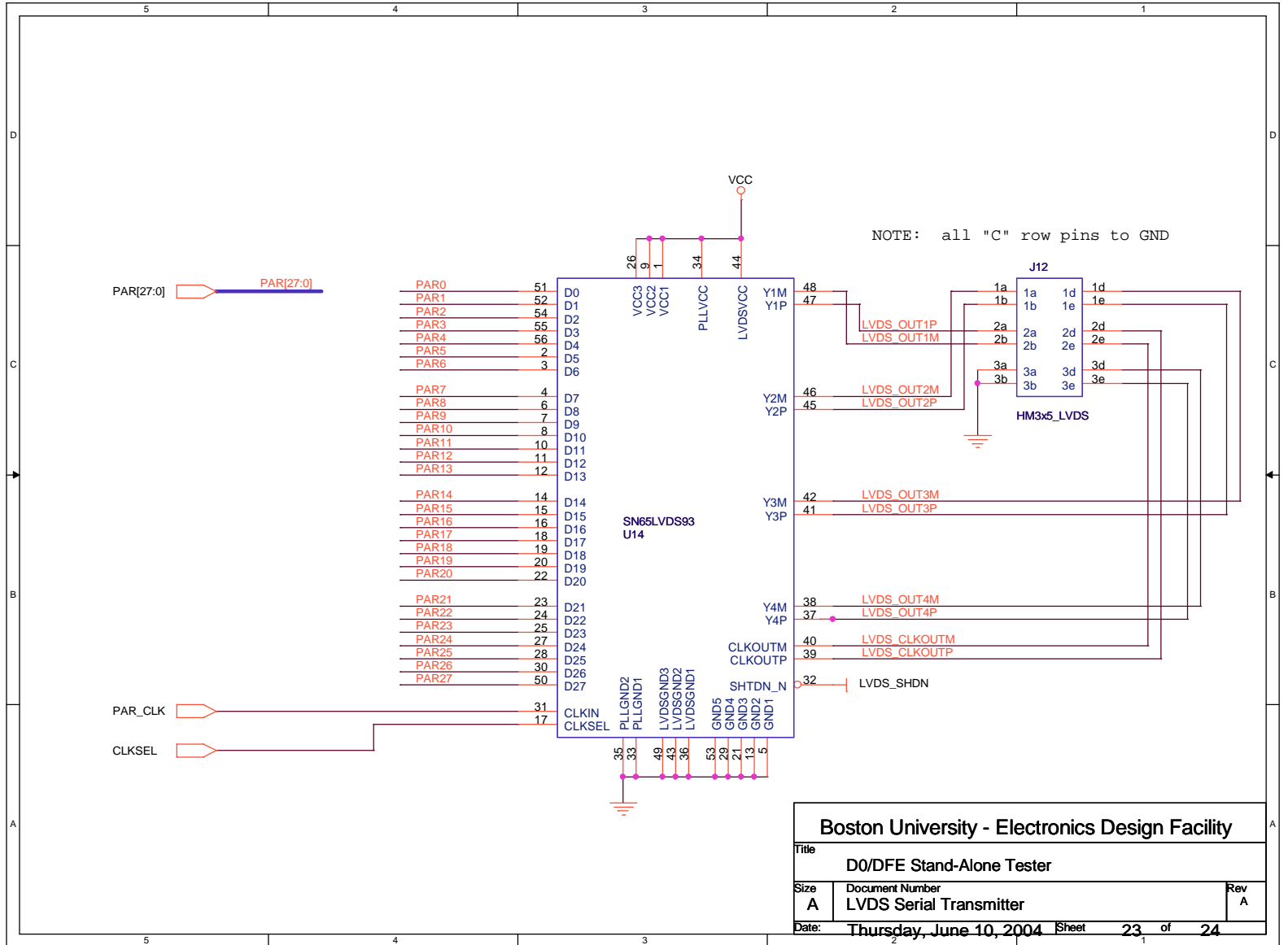
Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
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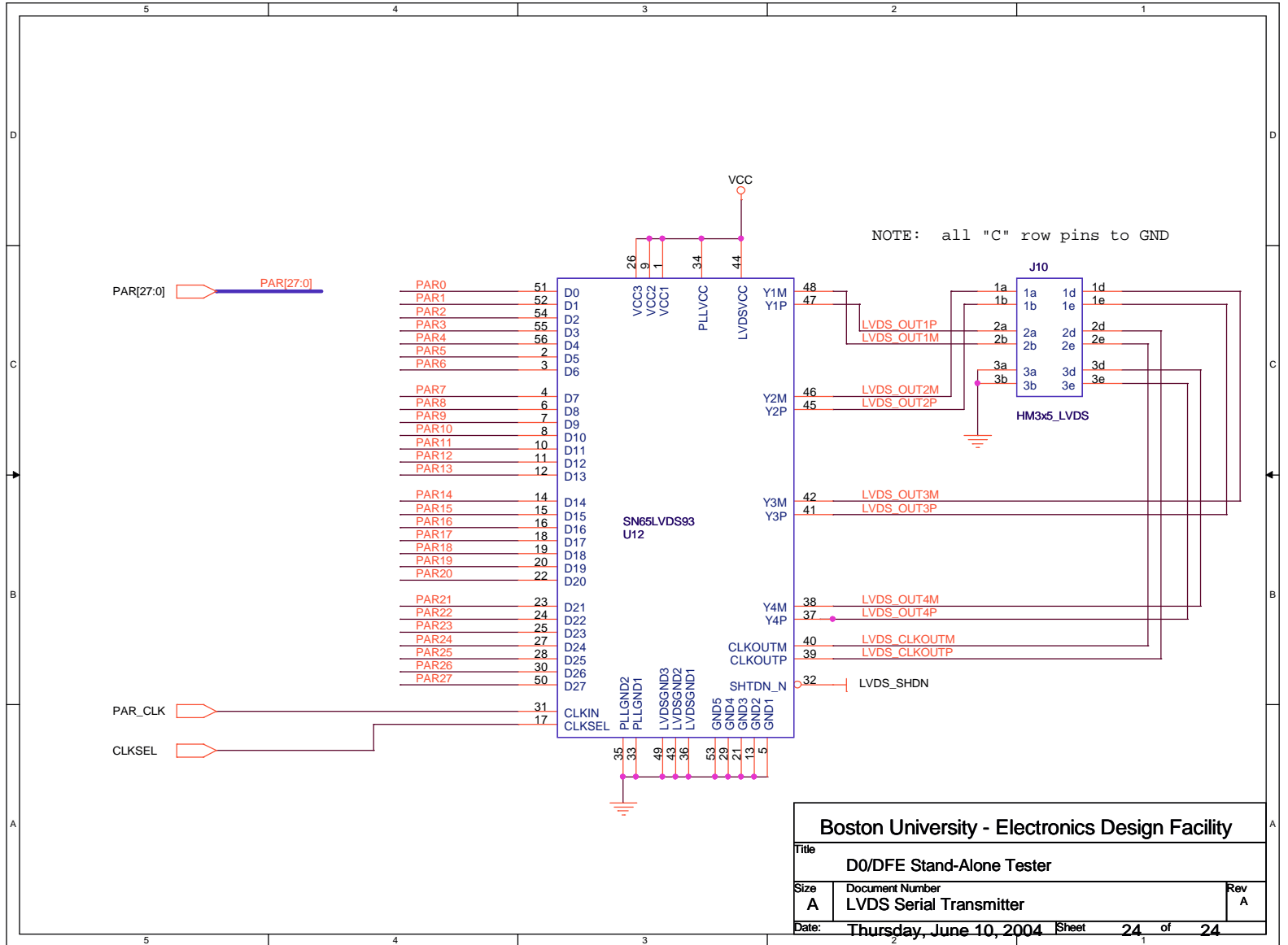
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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
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Title		
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Title		
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Title D0/DFE Stand-Alone Tester		
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