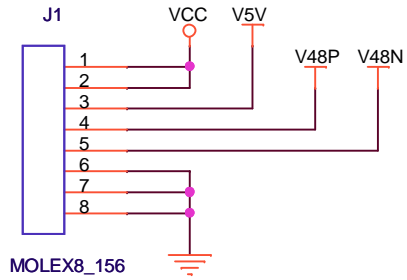


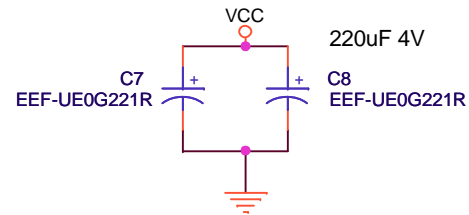
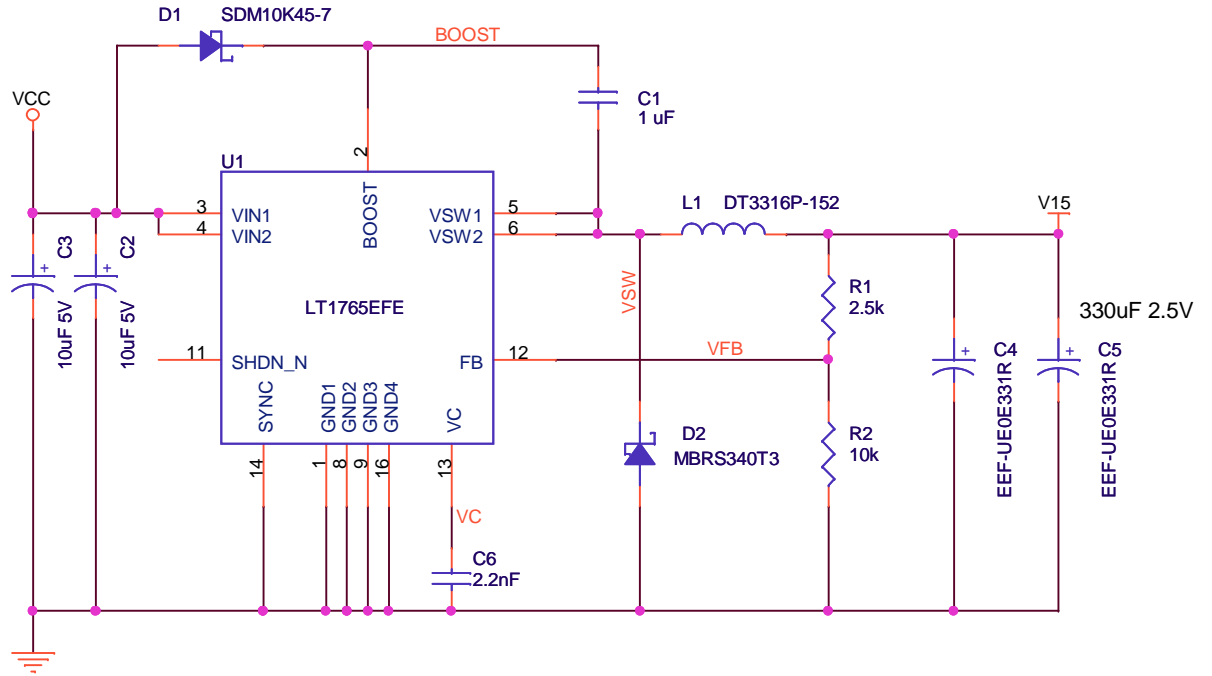
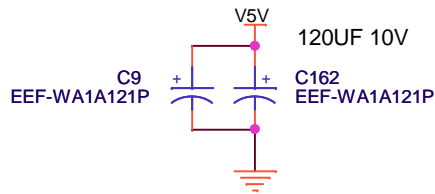
Title		
DSAT Tester Schematic		
Size	Document Number	Rev
Customer	Doc	<Rev Code
Date:	Monday, May 03, 2004	Sheet 1 of 24

1.5V FPGA core power regulator



LEGEND

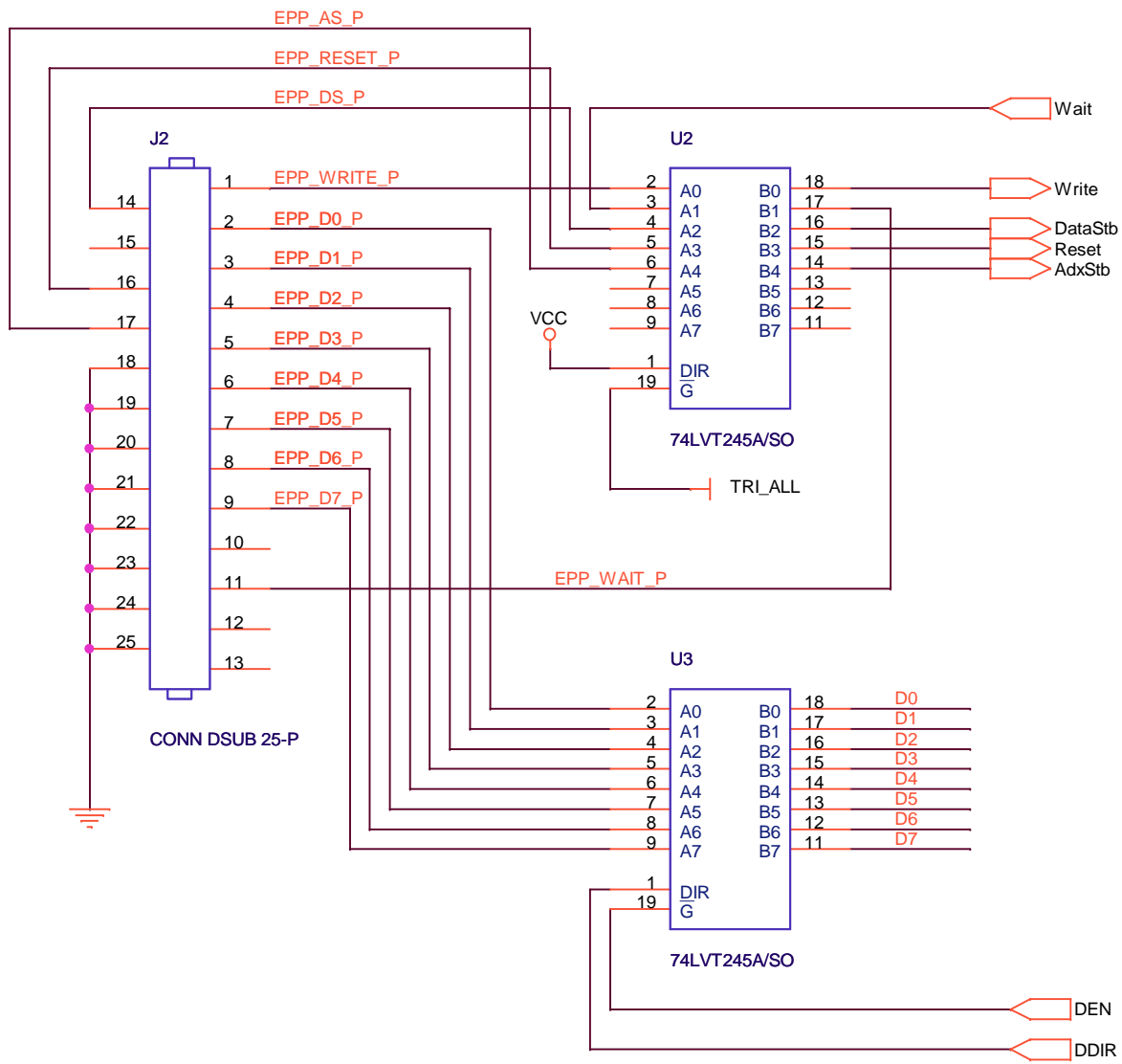
- 1 - 3.3V
- 2 - 3.3V
- 3 - 5V
- 4 - +48V
- 5 - -48V
- 6 - GND
- 7 - GND
- 8 - GND

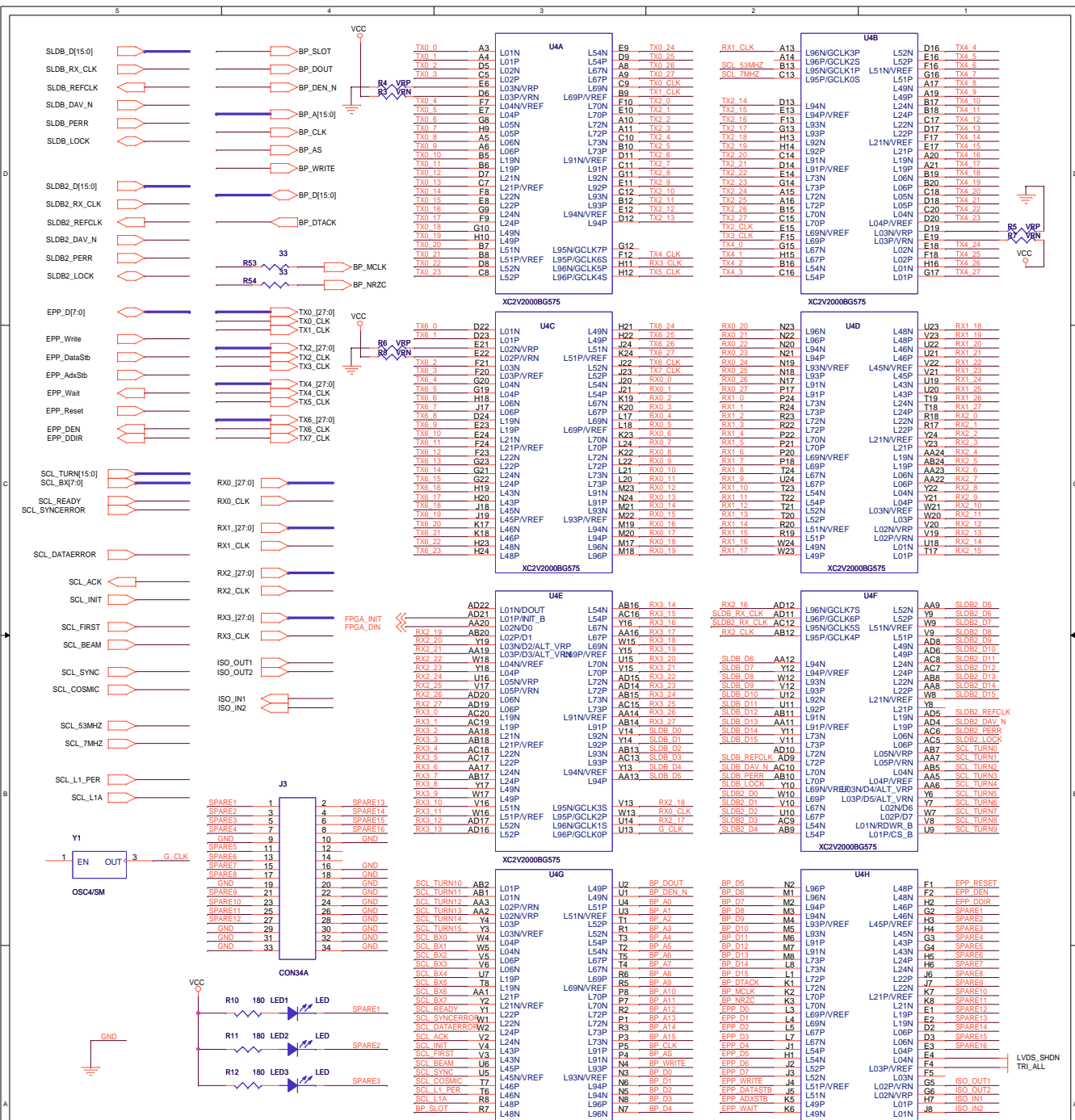


Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number Power Input	Rev A
Date: Thursday, May 06, 2004	Sheet 2	of 24



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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
	Bypass Capacitors	A
Date:	Thursday, May 06, 2004	Sheet 3 of 24





FPGA Pinout Notes:

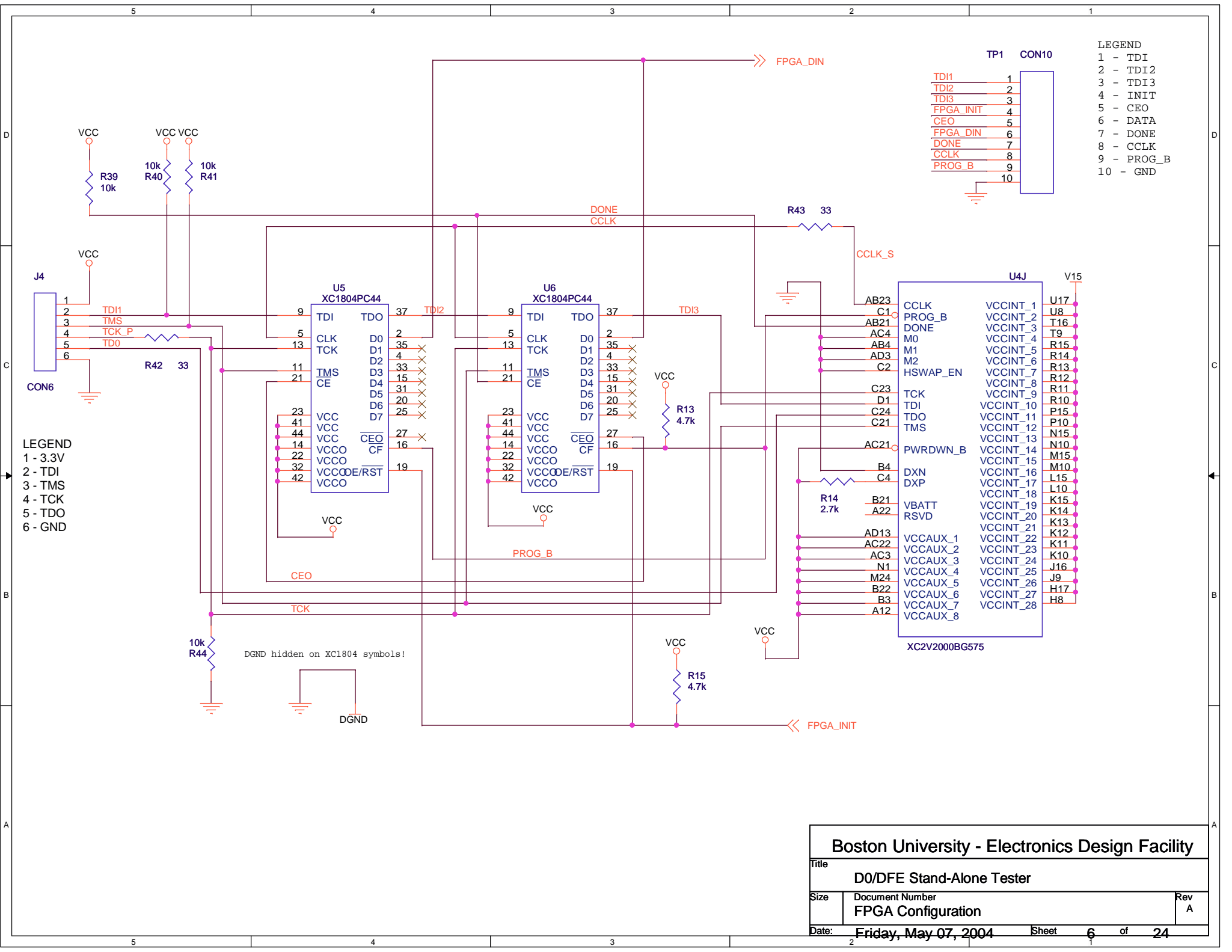
- Each symbol is one I/O bank
- Any bank with TX pins used must have resistors on VRP, VRN pins for impedance control
- The following must be on GCLKxP (primary clock) pins: G_CLK, RXn_CLK, SLDBn_RX_CLK, SCL_xxMHZ (8 total) [Otherwise, any necessary swapping should be OK]

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Title: **D0/DFE Stand-Alone Tester**

Size: **Document Number**
FPGA Signal Connections

Date: **Friday, May 07, 2004** Sheet: **5** of **24**



TP1 CON10

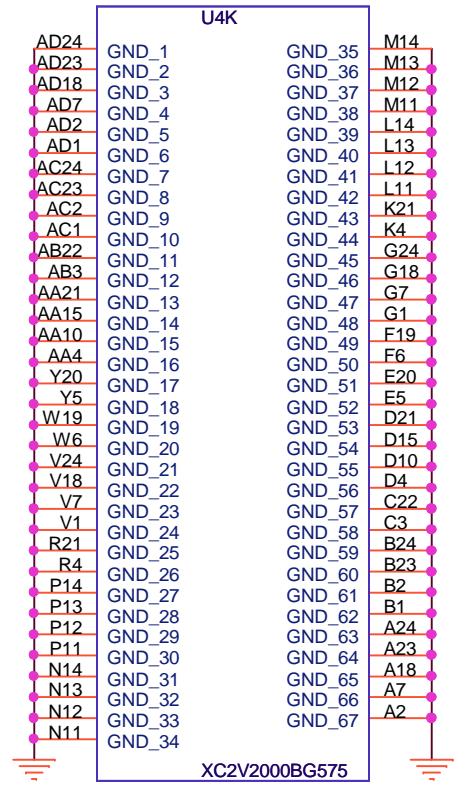
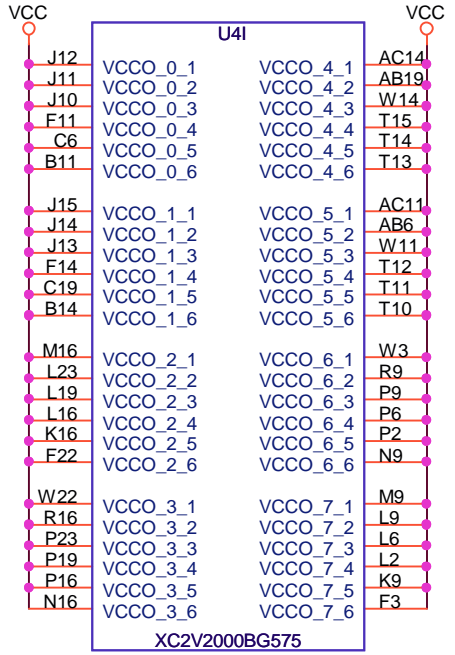
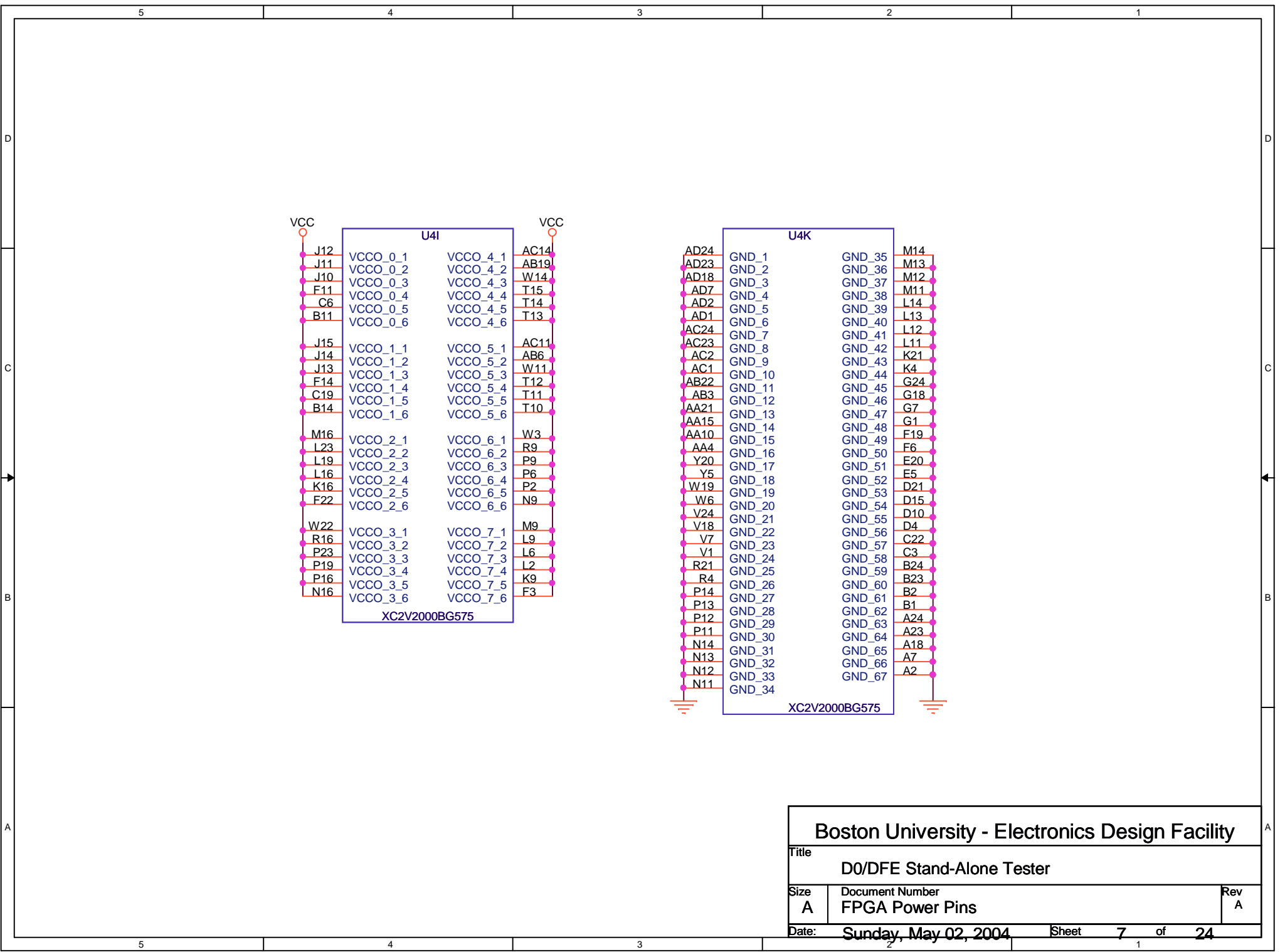
TDI1	1
TDI2	2
TDI3	3
FPGA_INIT	4
CEO	5
FPGA_DIN	6
DONE	7
CCLK	8
PROG_B	9
	10

- LEGEND
- 1 - TDI
 - 2 - TDI2
 - 3 - TDI3
 - 4 - INIT
 - 5 - CEO
 - 6 - DATA
 - 7 - DONE
 - 8 - CCLK
 - 9 - PROG_B
 - 10 - GND

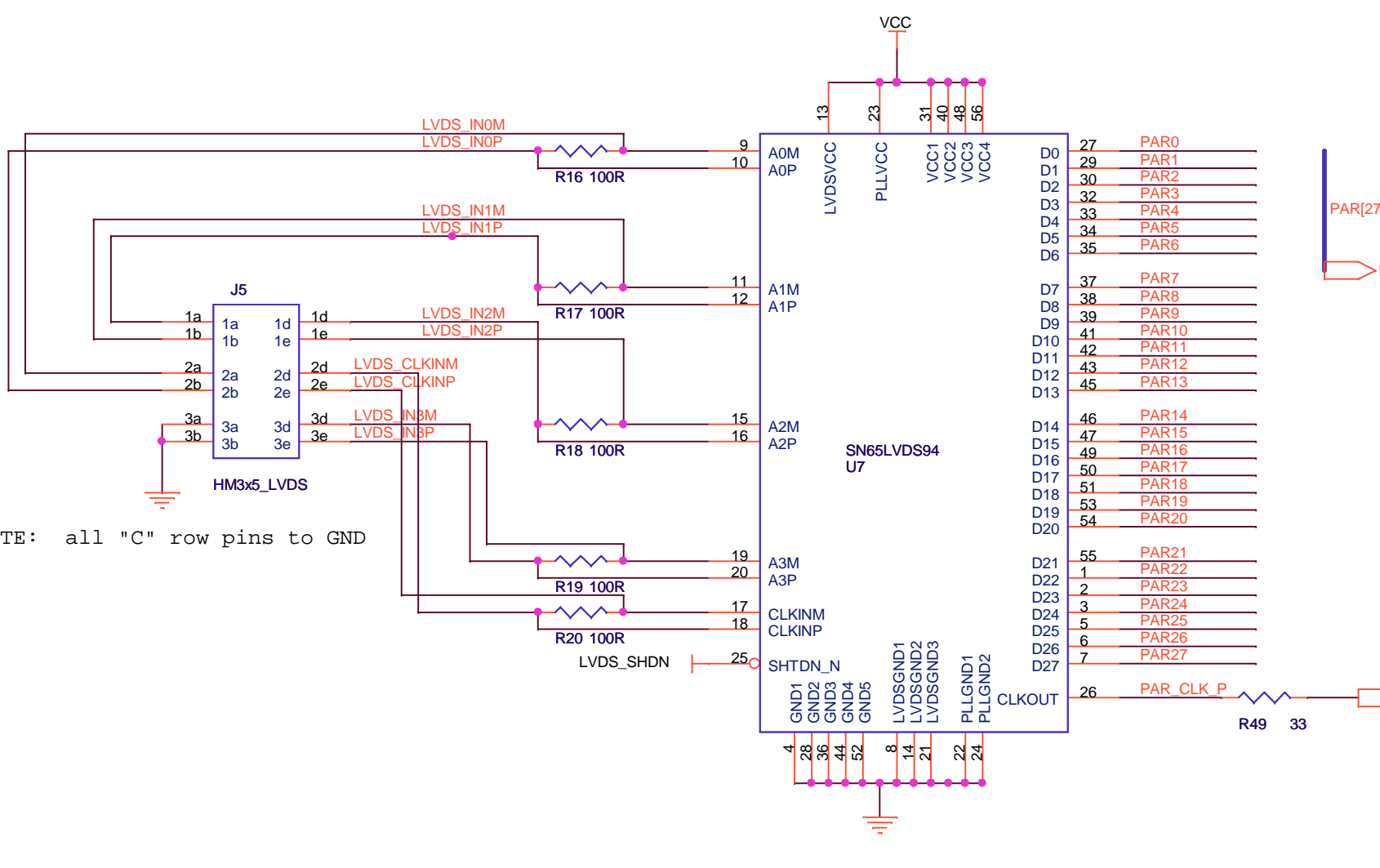
- LEGEND
- 1 - 3.3V
 - 2 - TDI
 - 3 - TMS
 - 4 - TCK
 - 5 - TDO
 - 6 - GND

DGND hidden on XC1804 symbols!

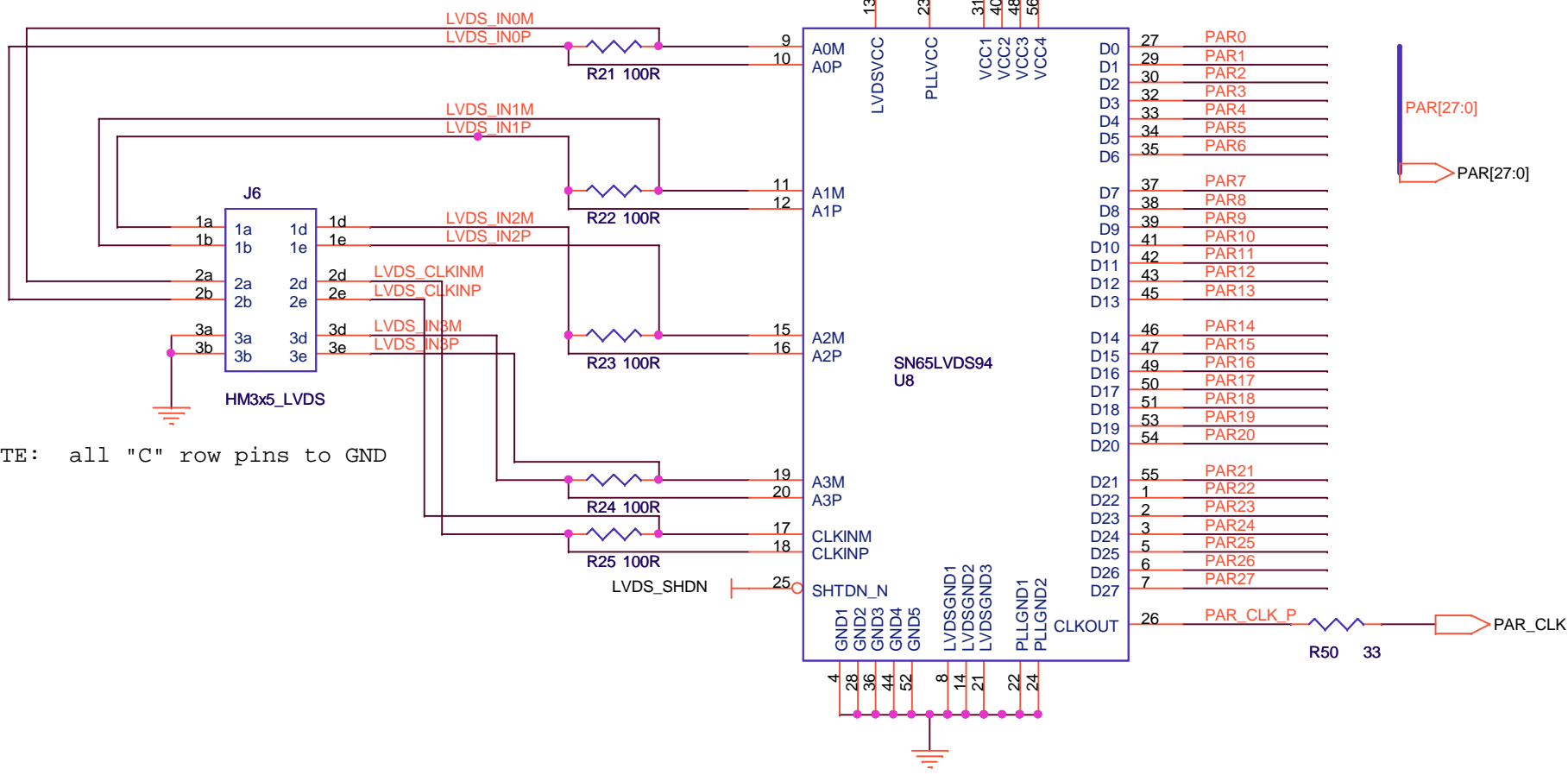
Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size	Document Number FPGA Configuration	Rev A
Date:	Friday, May 07, 2004	Sheet 6 of 24



Boston University - Electronics Design Facility		
Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	FPGA Power Pins	A
Date:	Sunday, May 02, 2004	Sheet 7 of 24

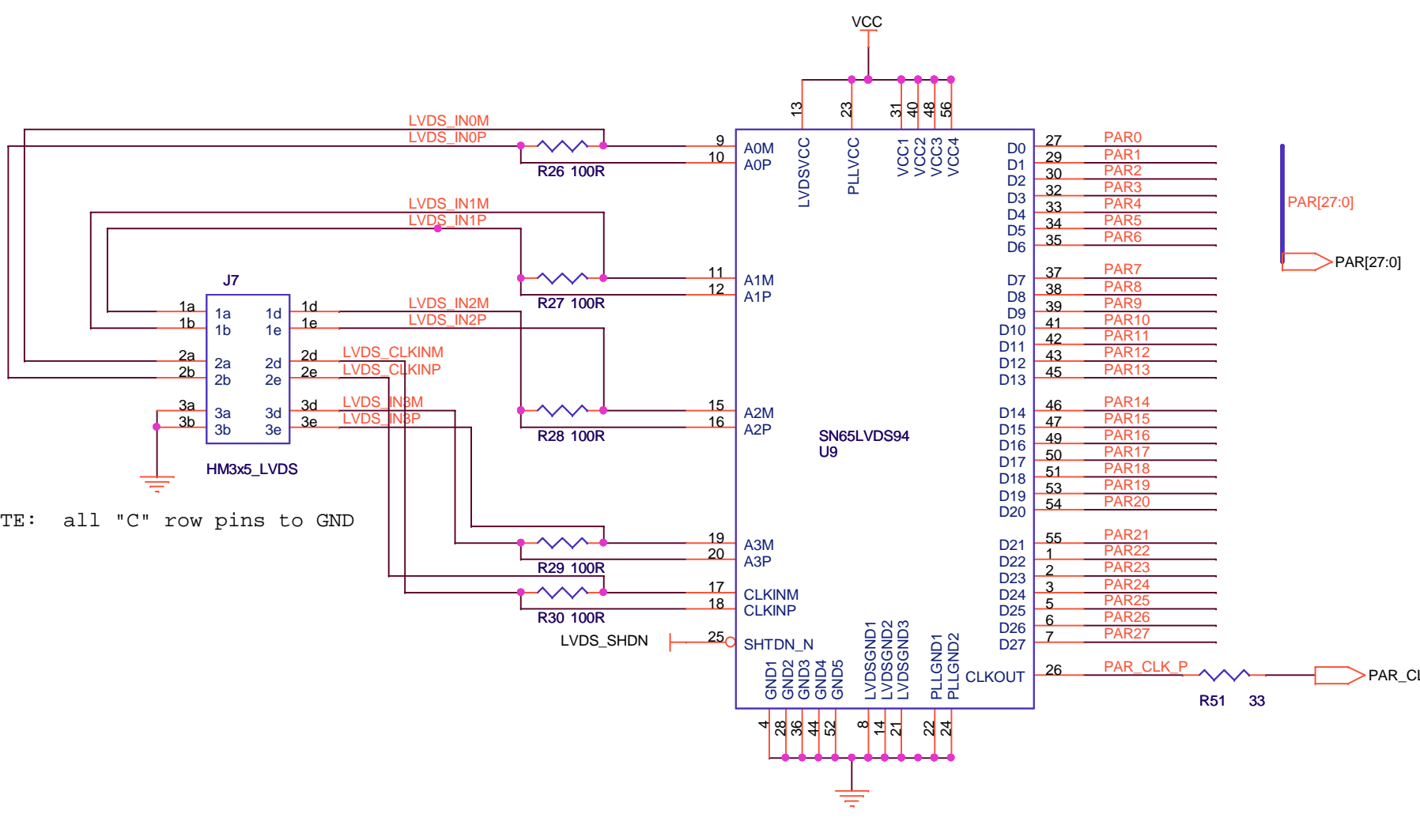


NOTE: all "C" row pins to GND



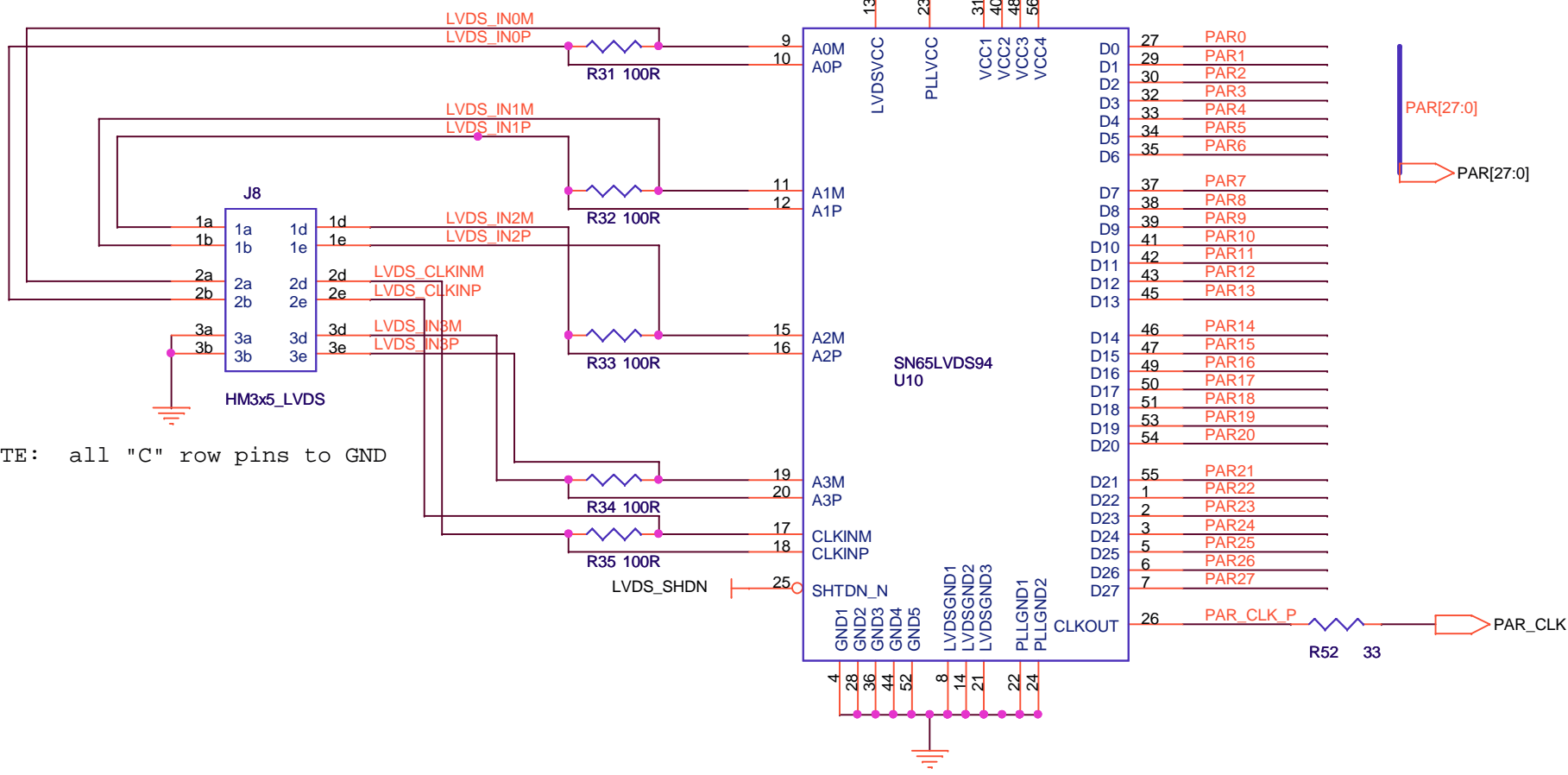
NOTE: all "C" row pins to GND

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Receiver	Rev A
Date: Friday, May 07, 2004	Sheet 9	of 24



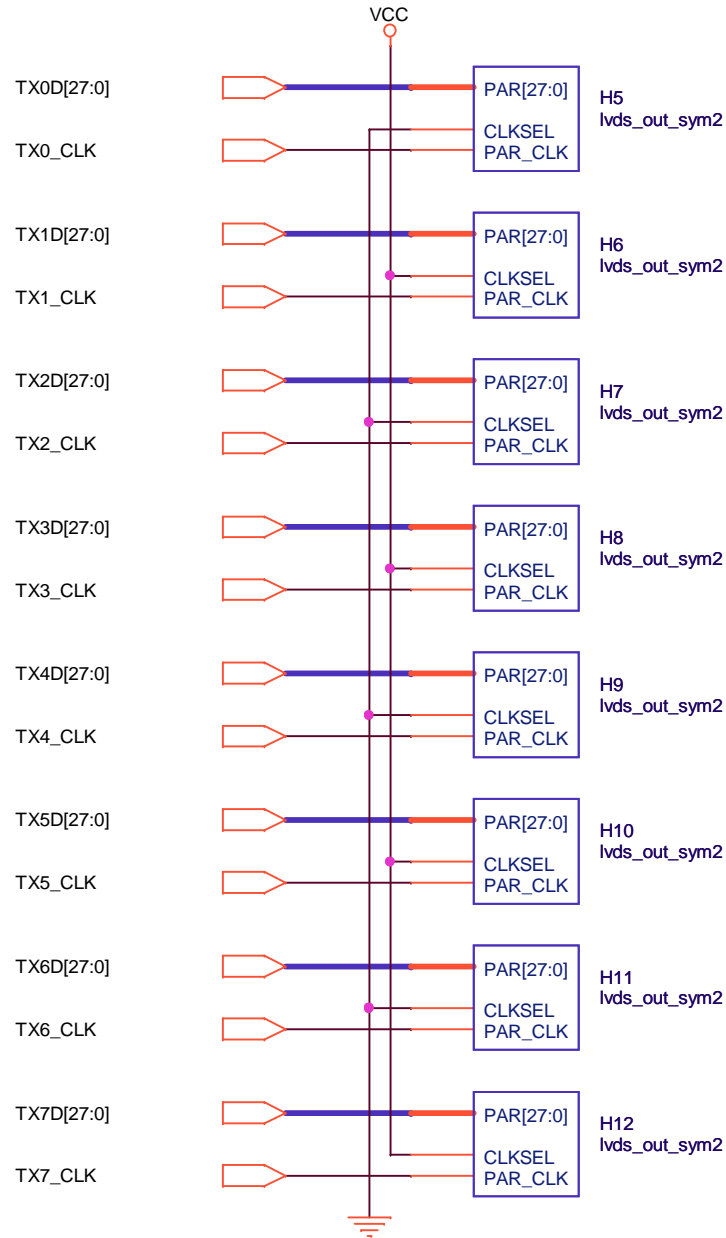
NOTE: all "C" row pins to GND

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Receiver	Rev A
Date: Friday, May 07, 2004	Sheet 10	of 24



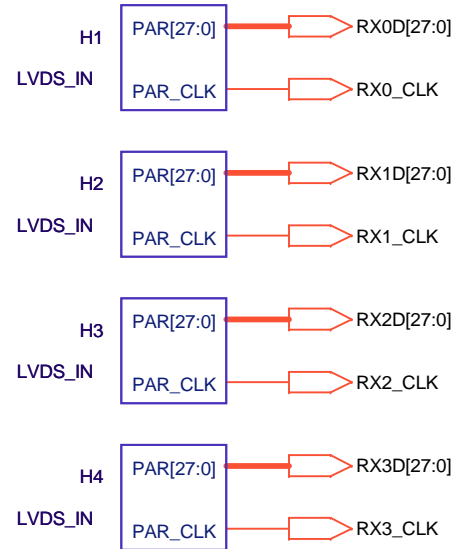
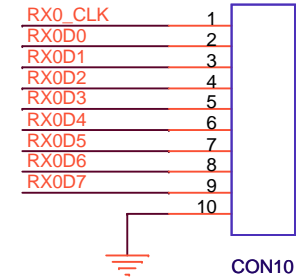
NOTE: all "C" row pins to GND

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Receiver	Rev A
Date: Friday, May 07, 2004	Sheet 11	of 24

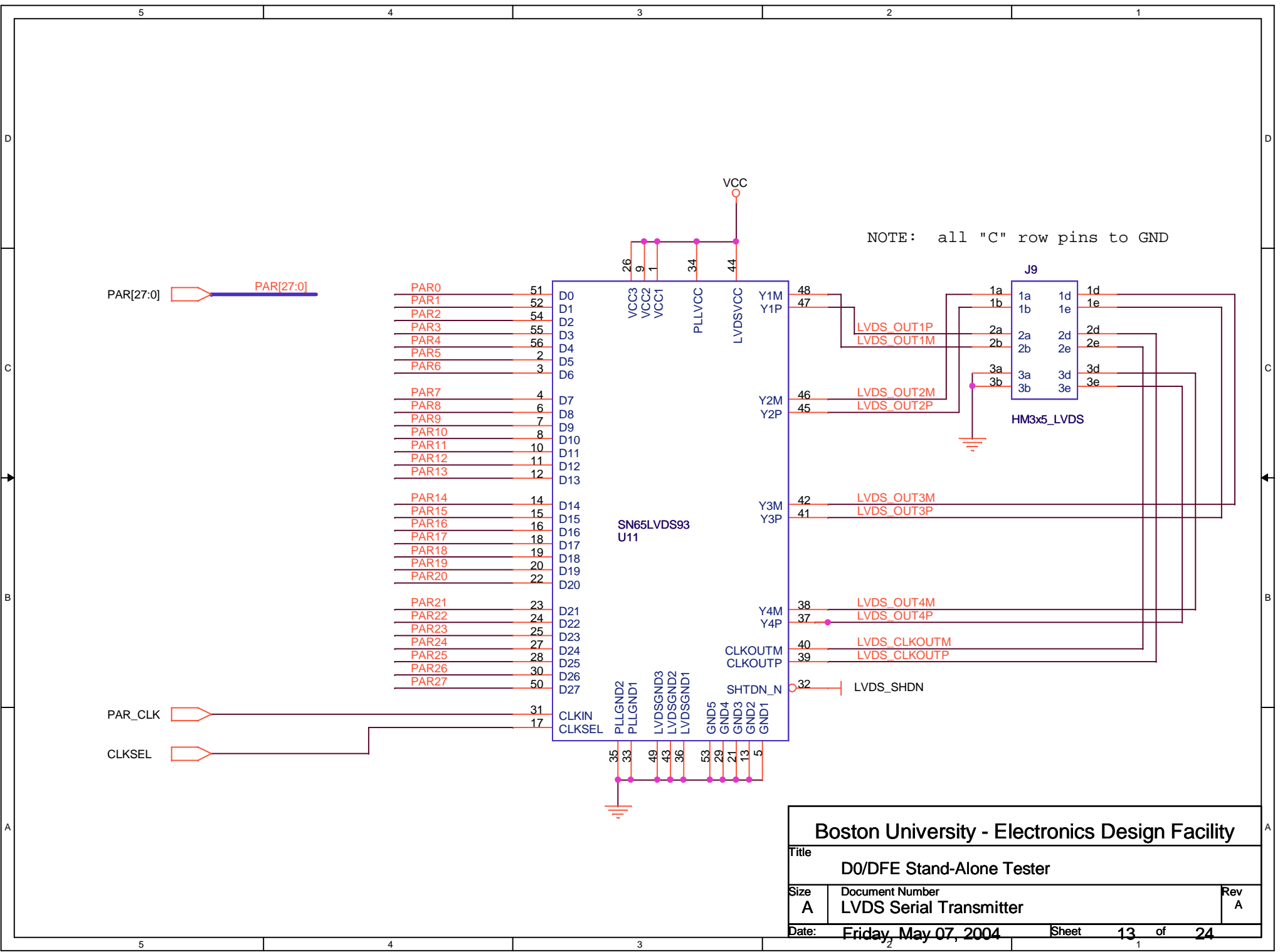


LEGEND

- 1 - RX0_CLK
- 2-9 - RX0[7:0]
- 10 - GND

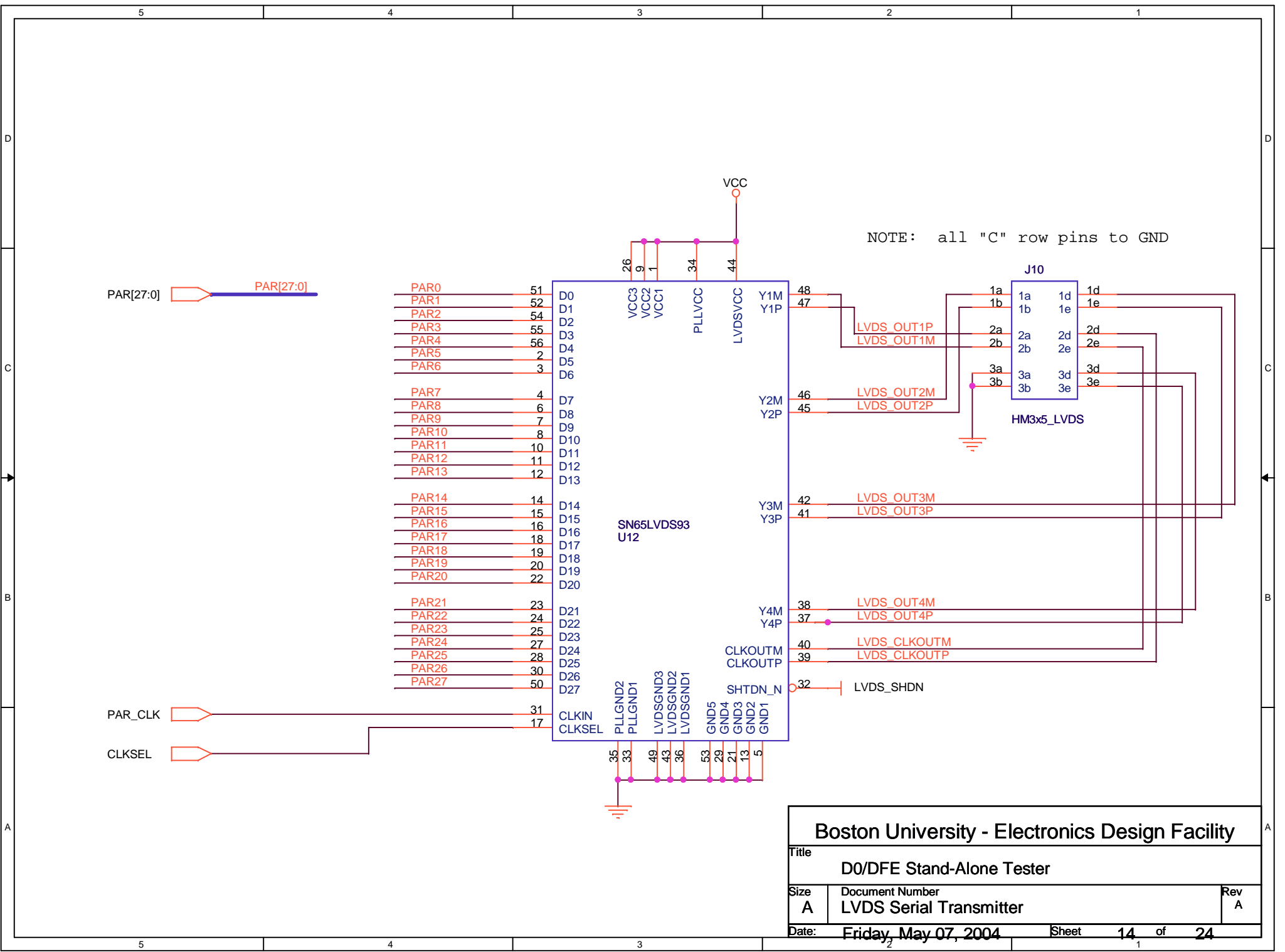


Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial I/O	Rev A
Date: Tuesday, May 04, 2004	Sheet 12	of 24

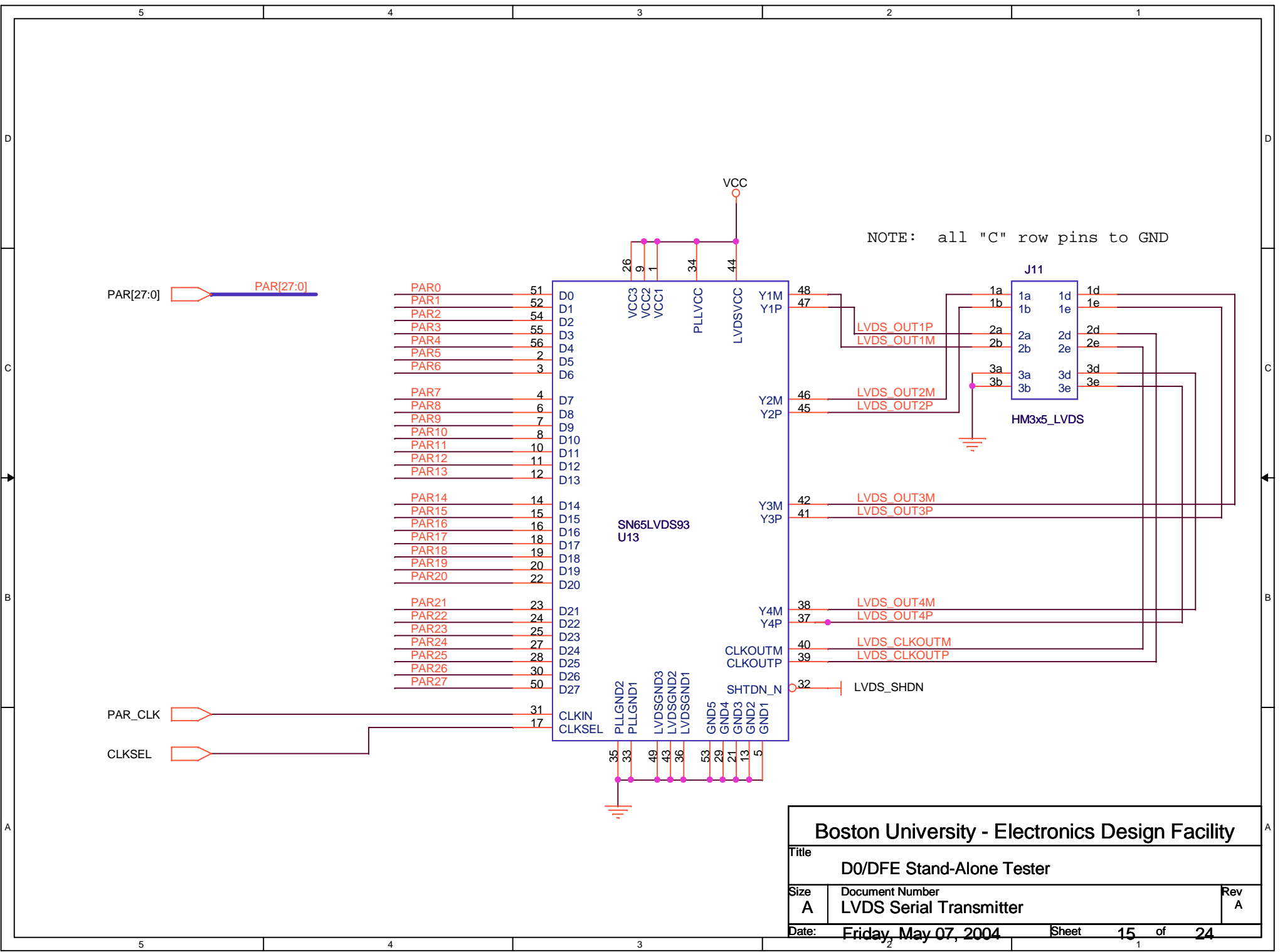


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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 13 of 24



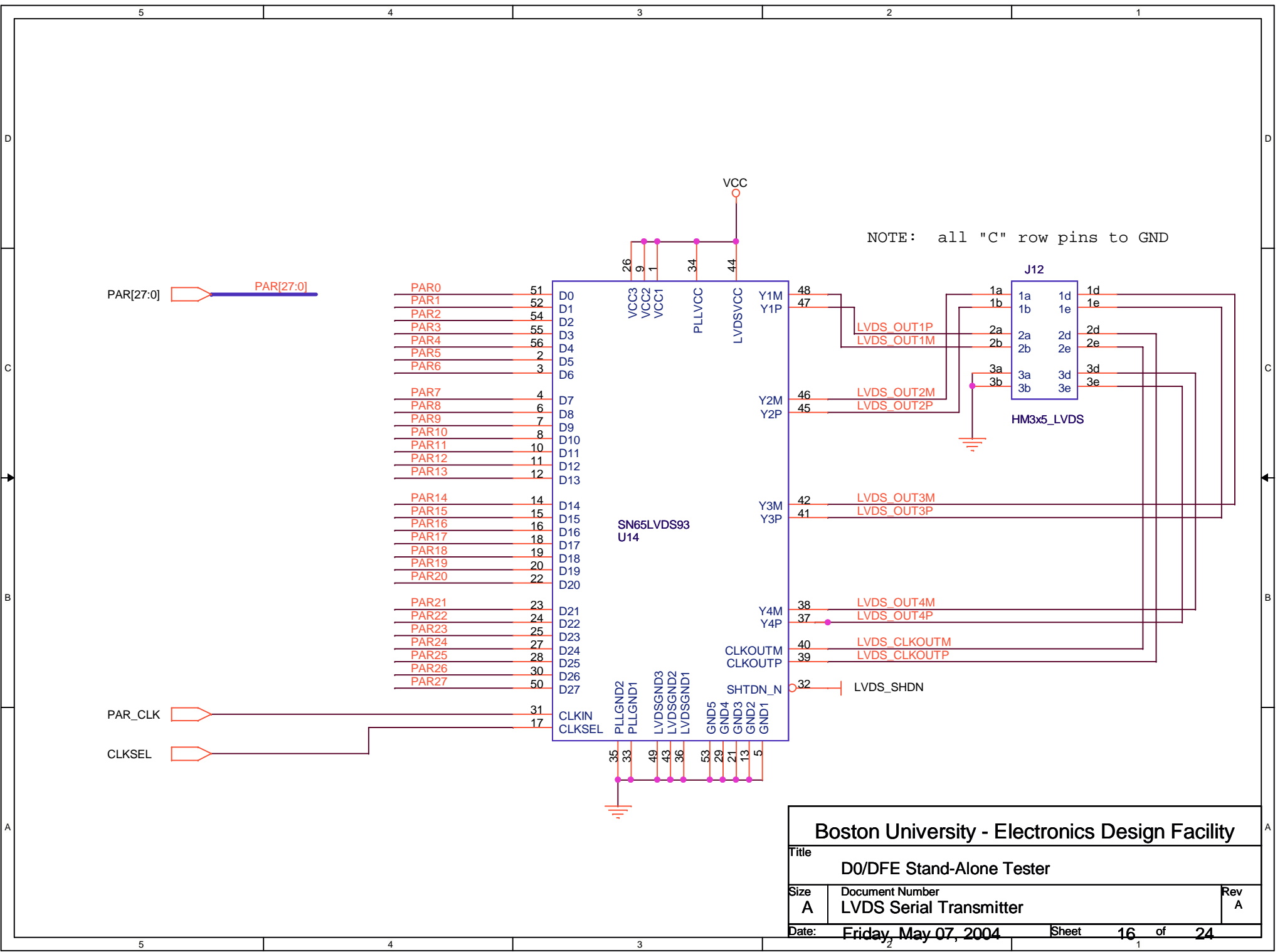
Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number LVDS Serial Transmitter	Rev A
Date: Friday, May 07, 2004	Sheet 14	of 24



NOTE: all "C" row pins to GND

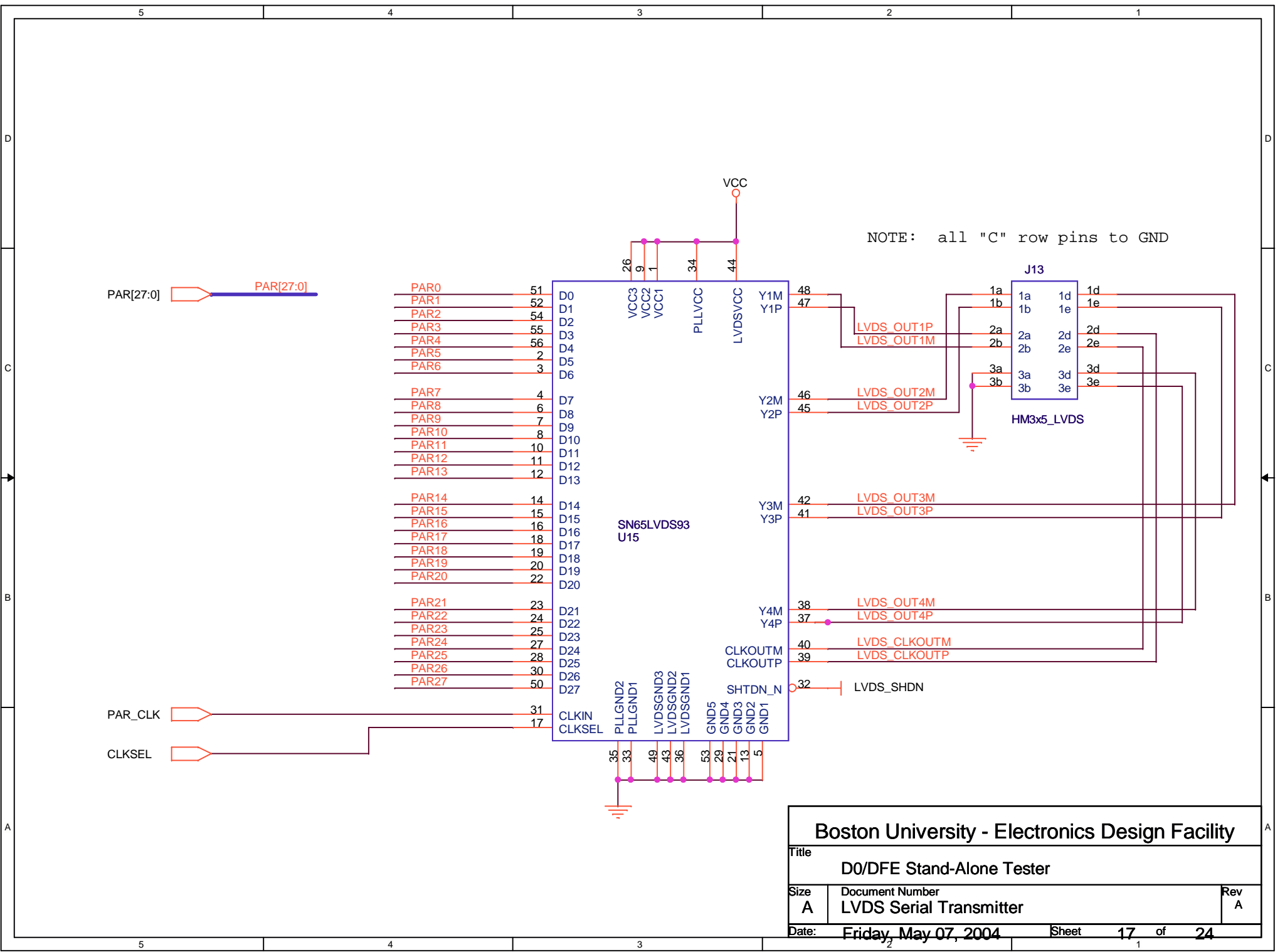
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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 15 of 24



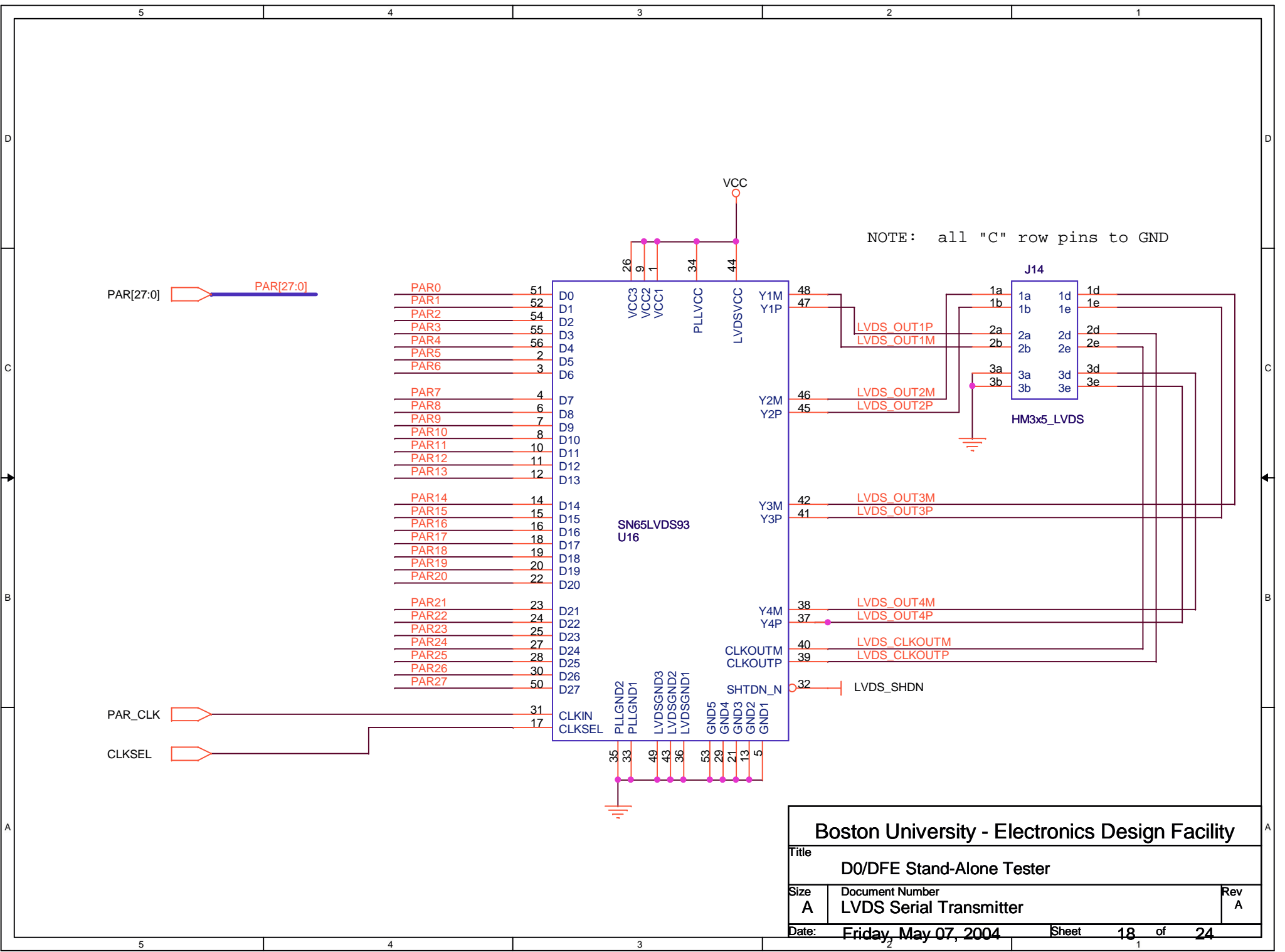
Boston University - Electronics Design Facility

Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 16 of 24



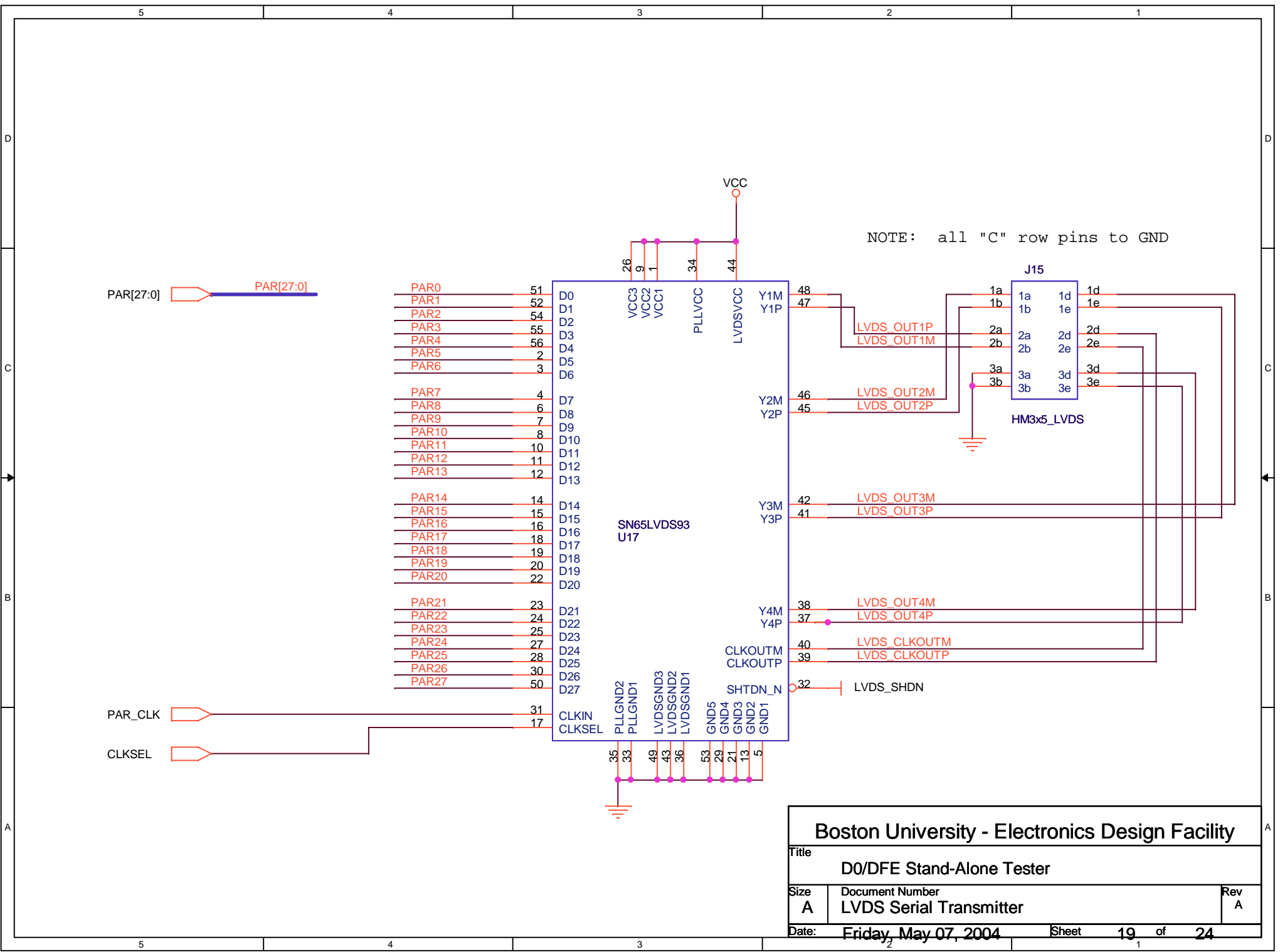
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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 17 of 24



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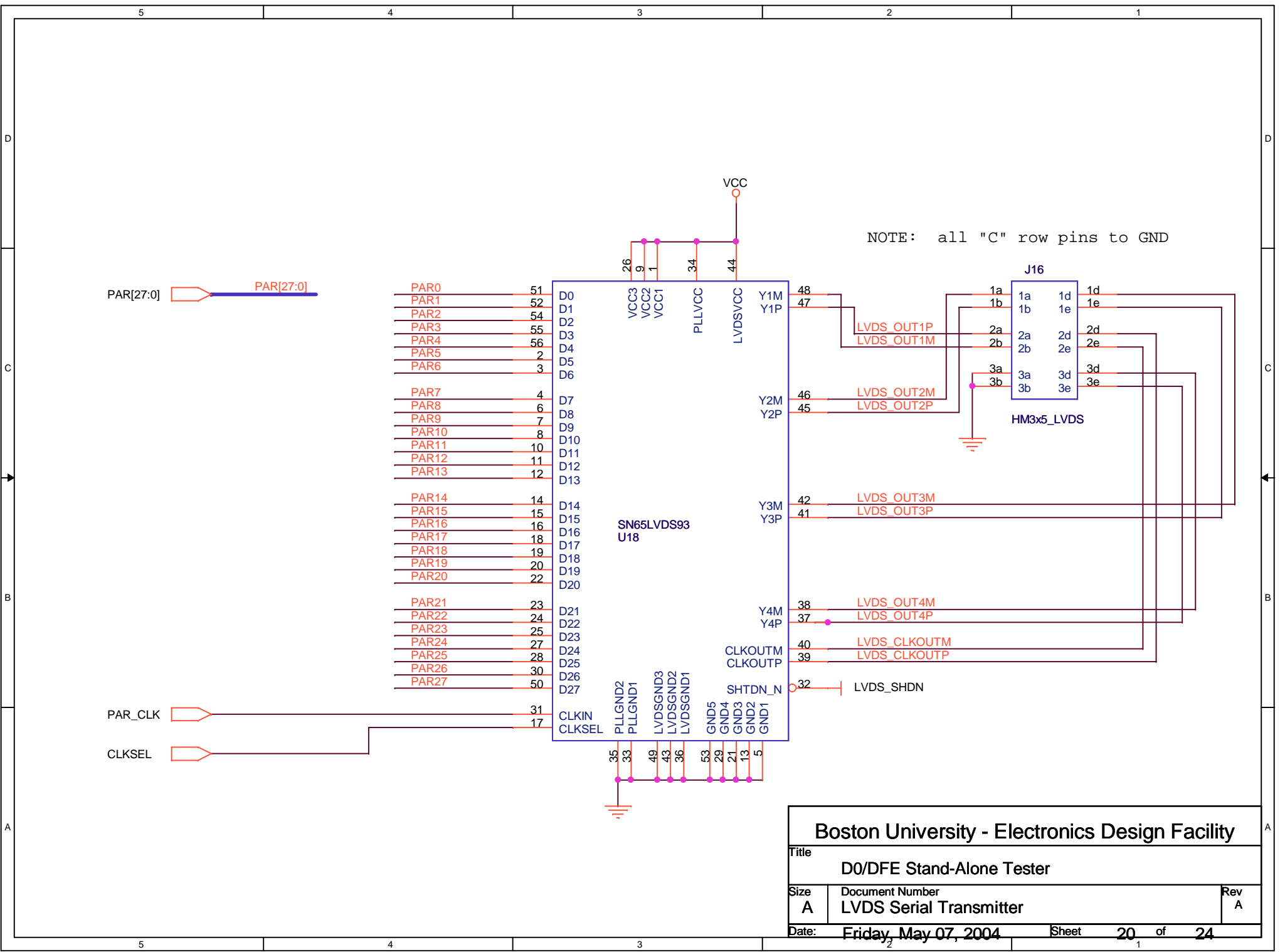
Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 18 of 24



NOTE: all "C" row pins to GND

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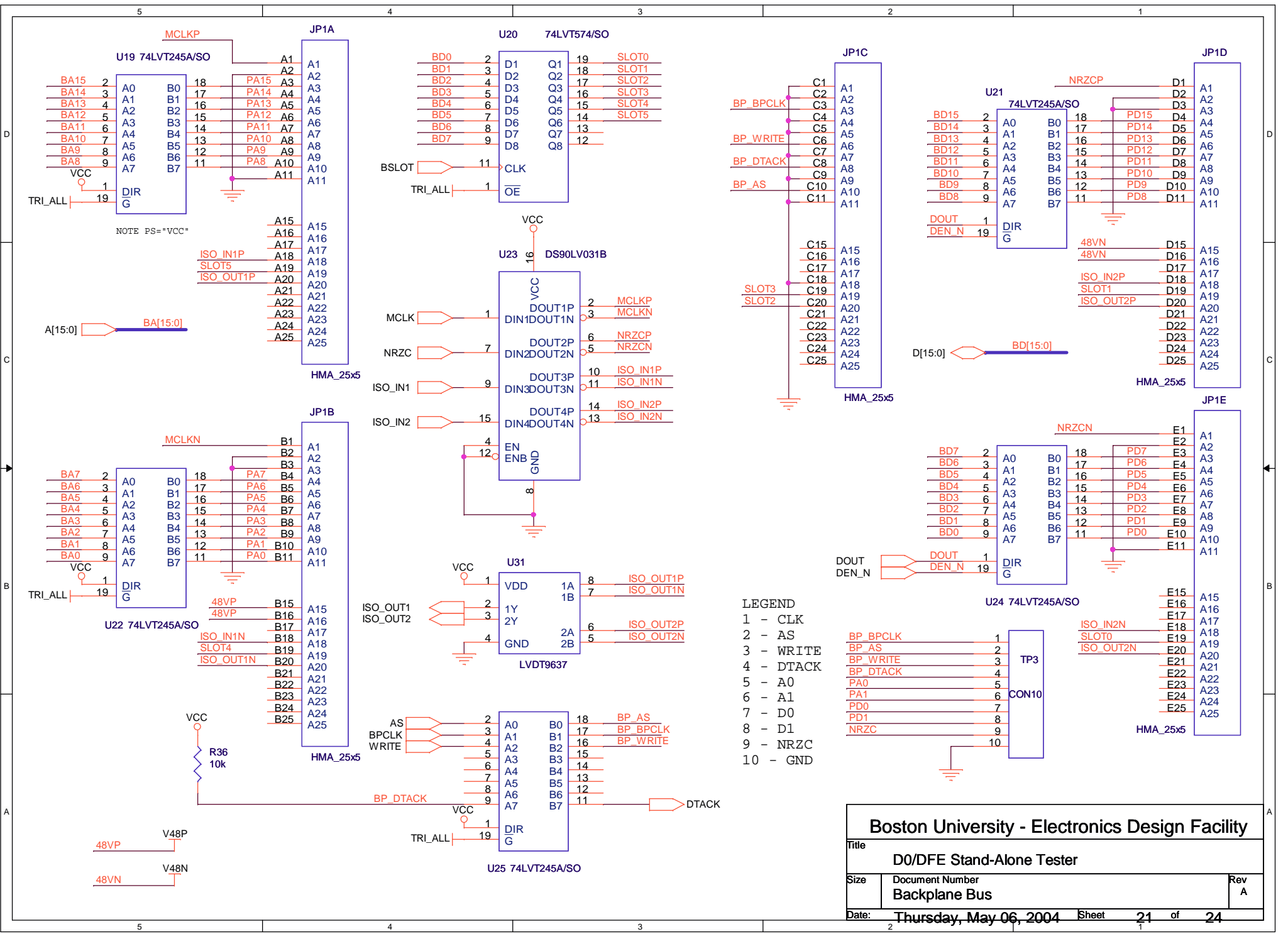
Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 19 of 24

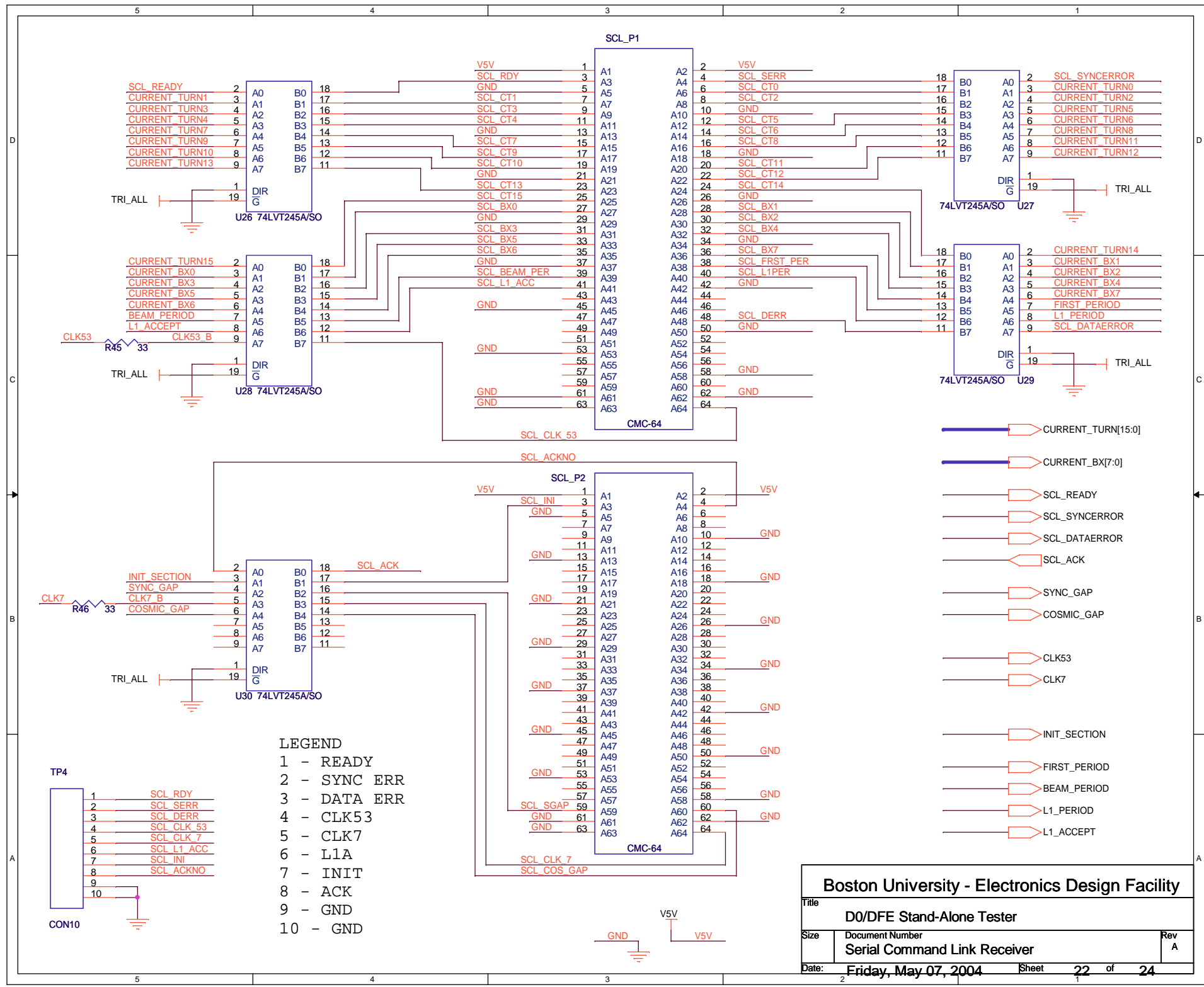


NOTE: all "C" row pins to GND

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Title		
D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
A	LVDS Serial Transmitter	A
Date:	Friday, May 07, 2004	Sheet 20 of 24

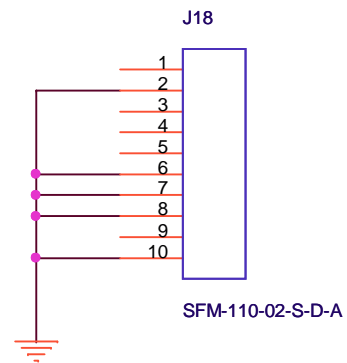
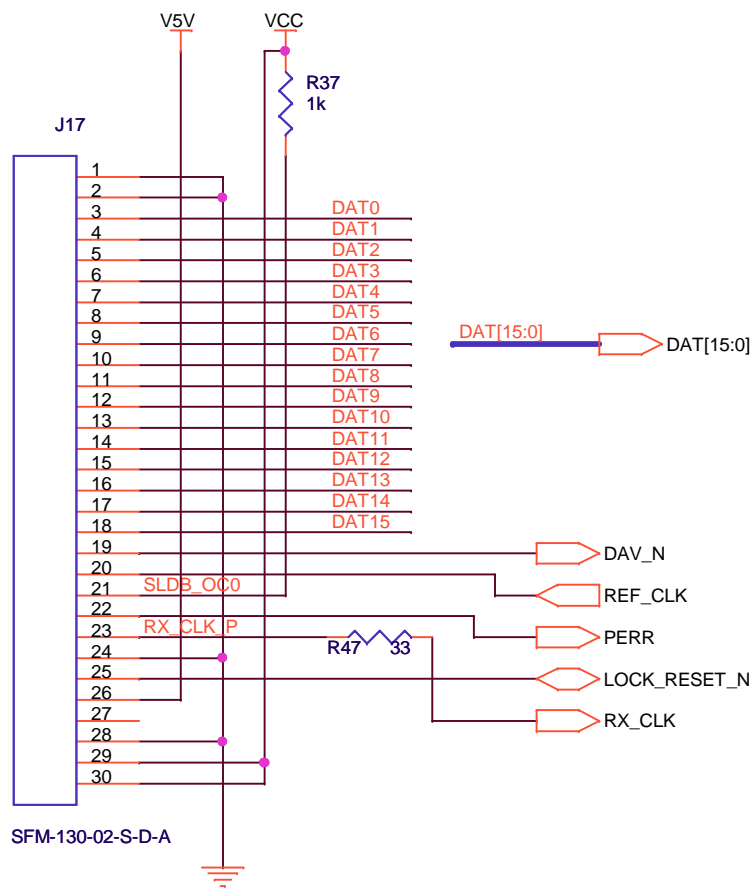




- LEGEND**
- 1 - READY
 - 2 - SYNC ERR
 - 3 - DATA ERR
 - 4 - CLK53
 - 5 - CLK7
 - 6 - L1A
 - 7 - INIT
 - 8 - ACK
 - 9 - GND
 - 10 - GND

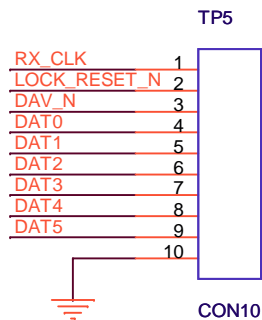
- CURRENT_TURN[15:0]
- CURRENT_BX[7:0]
- SCL_READY
- SCL_SYNCERROR
- SCL_DATAERROR
- SCL_ACK
- SYNC_GAP
- COSMIC_GAP
- CLK53
- CLK7
- INIT_SECTION
- FIRST_PERIOD
- BEAM_PERIOD
- L1_PERIOD
- L1_ACCEPT

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Title D0/DFE Stand-Alone Tester		
Size	Document Number	Rev
	Serial Command Link Receiver	A
Date:	Friday, May 07, 2004	Sheet 22 of 24



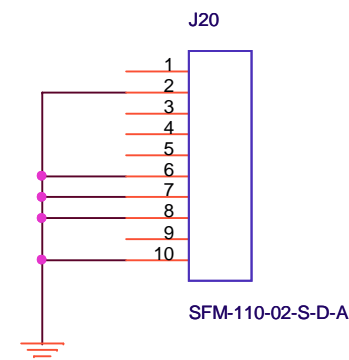
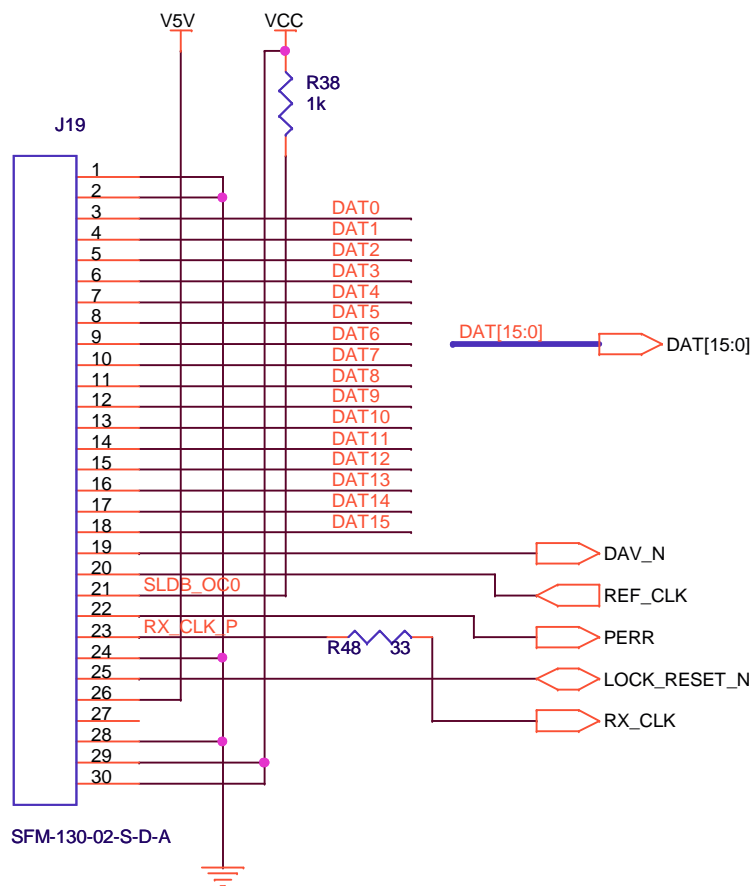
LEGEND

- 1 - RX_CLK
- 2 - LOCK
- 3 - DAV_N
- 4-9 - DAT[0:5]
- 10 - GND



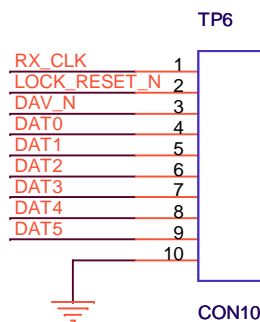
SLDB Serial Link Receiver
See spec sheet for connector placement

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number SLDB Serial Link Receiver	Rev A
Date: Friday, May 07, 2004	Sheet 23	of 24



LEGEND

- 1 - RX_CLK
- 2 - LOCK
- 3 - DAV_N
- 4-9 - DAT[0:5]
- 10 - GND



SLDB Serial Link Receiver
See spec sheet for connector placement

Boston University - Electronics Design Facility		
Title D0/DFE Stand-Alone Tester		
Size A	Document Number SLDB Serial Link Receiver	Rev A
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