1.5V FPGA core power regulator

**LEGEND**
- 1 - 3.3V
- 2 - 3.3V
- 3 - 5V
- 4 - +48V
- 5 - -48V
- 6 - GND
- 7 - GND
- 8 - GND
FPGA Pinout Notes:
- Each symbol is one I/O bank
- Any bank with TX pins used must have resistors on
  VPE, VRH pins for impedance control
- The following must be on GCLKxP (primary clock) pins:
  G_CLK, RX_CLK, SCLx_RX_CLK, SCLx_xMHz (8 total)
  [Otherwise, any necessary swapping should be OK]
NOTE: all "C" row pins to GND
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NOTE: all "C" row pins to GND
LEGEND
1 - RX0_CLK
2-9 - RX0[7:0]
10 - GND
NOTE: all "C" row pins to GND
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LEGEND
1 - RX_CLK
2 - LOCK
3 - DAV_N
4-9 - DAT[0:5]
10 - GND

SLDB Serial Link Receiver
See spec sheet for connector placement
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LEGEND
1 - RX_CLK
2 - LOCK
3 - DAV_N
4-9 - DAT[0:5]
10 - GND

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