1.5V FPGA core power regulator

**LEGEND**

1 - 3.3V
2 - 3.3V
3 - 5V
4 - +48V
5 - -48V
6 - GND
7 - GND
8 - GND
Rev B - 4/12/05, esh - add EPP series R's
FPGA Pinout Notes:
- Each symbol is one I/O bank
- Any bank with TX pins used must have resistors on VEP, VRH pins for impedance control
- The following must be on GCLKxP (primary clock) pins:
  - G_CLK, Rn_CLK, SLSn_RX_CLK, SCL_xMHS (8 total)
  [Otherwise, any necessary swapping should be OK]

4/11/05, esh - Rev B: Exchange R6, R8
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
**LEGEND**

1 - RX0_CLK
2-9 - RX0[7:0]
10 - GND

**Diagram Description**

- Connection points labeled with numbers (1-10).
- Signal labels: RX0_CLK, RX0[7:0], GND.
- Each connection point is marked with a corresponding number for identification.
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
NOTE: all "C" row pins to GND
Note: all "C" row pins to GND
NOTE: all "C" row pins to GND
LEGEND
1 - RX_CLK
2 - LOCK
3 - DAV_N
4-9 - DAT[0:5]
10 - GND

SLDB Serial Link Receiver
See spec sheet for connector placement

Boston University - Electronics Design Facility
Title: D0/DFE Stand-Alone Tester
Size: A
Document Number: SLDB Serial Link Receiver
Date: Tuesday, June 08, 2004
Sheet 23 of 24
LEGEND
1 - RX_CLK
2 - LOCK
3 - DAV_N
4-9 - DAT[0:5]
10 - GND

SLDB Serial Link Receiver
See spec sheet for connector placement