

Modifications to DSAT in Rev. 9

RW_BUS

1. Slot number register initialized to 0 at power up.
2. Configuration data are written using all 4 bytes to speed it up.

SCL

1. Tick and Turn counts are locally implemented as inside DFEA2 and they are synchronized upon receiving SCL reset.
2. SG and FX signals are generated at Tick locations as specified by D0 experiment.
3. Only four bits are used in each SCL buffer word:
 - Bit 0 level 1
 - Bit 1 SCL reset
 - Bit 2 ISO_IN0
 - Bit 3 ISO_IN1
4. SCL buffer address is incremented every seven clock cycles during transmission.
5. scl_wcount reduced to eight bits. Each count represents one event (seven clocks), correspondingly, the local address is also reduced to eight bits. Tick and turn counter values of the first triggered event is latched and could be read out at address 3, where bit 7-0 is scl_wcount, bit 15-8 is latched Tick number and bit 31-16 is latched Turn number.
6. Control bits overwrite the corresponding Link data (Tx outputs) bits to guarantee correct embedded control bits.
7. SCR bits are now;
 - Bit 0 enable bit
 - Bit 1 busy bit
 - Bit 2 trigger bit
 - Bit 3 trigger on specified Tick enable bit
 - Bit 4 enable directly pass Rx ports to Tx ports (BER test)
 - Bit 5 enable sending DFEA Link pattern
 - Bit 6 not used
 - Bit 7 system reset
 - Bit 8-15 Tick number to be triggered on (write only, there is an offset)
 - Bit 16-31 Repeat count (write only)
(0 = trigger once, n = repeat trigger every n*7 clocks)
8. Signals are delayed in a way that Level 1, SCL reset and ISO_IN signals in the first SCL buffer word are properly aligned with Link data of the first event in Tx buffers.

LVDS_tx

1. When repeated trigger is enabled (CSR bit 5 = 1), there will be no gap in consecutive triggers.
2. As specified in SCL sector, sending pattern and direct feed through of LVDS_rx data features have been added.

LVDS_rx

1. Delay register reduced to 7 bits. The delay unit is event instead of clock.
2. Automatic alignment to CTOC Level 1 header.
3. Receiver data expanded to 32 bits. Bit 28 is data valid flag. Bit 31 is ISO_OUT0 (rx0 and rx1) or ISO_OUT1 (rx2 and rx3). Bit 29 is ISO_OUTx before synchronization.

SLDB_rx

1. Receiver data bits 15-0 are muon data. Bit 16 is parity error from SLDB. Bit 17 is DAV signal from SLDB. Bit 31 is a valid bit from DSAT.
2. CSR bits 4-0 are the same as LVDS_rx. Bit 5 is SLDB reset which is needed for example after a DSAT reconfiguration. Bit 6 is '1' if parity error has been seen while DAV is '1'. Bit 7 is SLDB LOCK status.
3. Delay register is 7 bits only. Unit is event.
4. Automatic alignment to first MUON track word.

All delay settings of DSAT are optimized at current test setup. Timing difference caused by LVDS cable length or silicon delay in DSAT/DFEA2 within plus/minus three clock cycles could be tolerated.