Managing the Word Count

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The word count read back to VMEbus indicates the number of 64 bit words available for readout. For the test or oscilloscope modes, this count is equal to twice the number of FIFO words, four bytes contained in each FIFO word. For the triggered modes, the time word is also contained in the word count, so the word count is equal to twice the number of FIFO words plus the number of data blocks that have been written.

When writing to the FIFO in the triggered mode, it is important that complete data blocks be written, which means that there must be enough space in the FIFO when the write operation is started for the complete data block. This means that the actual number of written FIFO word pairs must be known and compared with the data block length before allowing a data block to be written. In other words, both the word count available to VMEbus (total word count) plus the FIFO word count must be retained in count registers. In the WFD these are called the total count and the FIFO count.

As words are written to the FIFO, both the total count and the FIFO count are incremented, except that when a new data block is written the total count must be incremented twice so as to include the time word. When words are read back to VMEbus, both counts are decremented except that when the time word is read, the FIFO count remains unchanged.

Normally up-down counters could be used for the total count and the FIFO count, but because these counters are operating at 125 MHz, where an up-count might need to be immediately followed by a down-count, there is insufficient time for the logic of a standard up-down counter to change from up to down within one clock cycle. Thus, instead of actually using up-down counters, the counters are each implemented using an adder and a subtractor plus a storage register. The incremented and decremented values
of the count are always available so the difference between an up-count and a down-count only depends on selecting the already available incremented or decremented value.

In the WFD where the total count sometimes needs to be incremented by two, an additional adder is used. Figure 1 shows the logic for the total count. The count register is implemented via a latched multiplexer using a select input signal to choose amongst no-change, incrementing, decrementing or double incrementing. A reset signal is also allowed in order to clear the counter when the FIFO is cleared.

A comparator compares the total count to zero so that one can tell when the total word count is zero and no further words should be read over VMEbus.

The logic for the FIFO count is shown in Fig 2. The counter proper is the same as for the total count, except that the latched multiplexer only has three possible inputs, no-change, increment or decrement.

A comparator indicates when the FIFO is empty.

An additional subtractor and comparator are included to indicate when the FIFO would have insufficient space for a new data block to be written.

The logic shown herein is replicated for each of the four channels and resides in BGA1M and BGA1S.

What is not shown here is an additional incrementer located in BGA2 that is used to indicate to VMEbus that an extra word is available for readout. In order to maintain the highest possible readout rate for 64 bit block transfers, a single word lookahead procedure is used in BGA2. Once a block transfer is started, there is always an extra word retained in BGA2 so that succeeding block transfers do not need to wait while data is fetched from BGA1M or BGA1S. Since this prefetched data has already been read from BGA1M or BGA1S, neither of these FPGA’s know that there is an unread word residing in BGA2, so BGA2 uses its incrementer to add one to the total count read from BGA1M or BGA1S. Once all words have been read to VMEbus, there is no longer any prefetched word in BGA2 and the incrementer is disabled.
Fig. 1 Logic for generating the total count
Fig. 2 Logic for generating the FIFO count