A 4 Channel 500 MHz Waveform Digitizer
(WFD)

William E. Earle

June 22, 2005

1 Overview

This document describes the structure and operating principles of a 4 channel 500 MHz waveform digitizer. The waveform digitizer is designed to digitize 4 channels of analog signals at a 500 MHz rate and to save the digitized data in FIFOs for subsequent readout via VMEbus.

Fig.1 shows the basic structure of the waveform digitizer, or WFD, a VME-based circuit board controlled by logic in three FPGAs. One of the FPGAs manages the interfacing to the VMEbus while each of the other FPGAs manages the data acquisition for two channels. Each input channel uses a small amount of analog circuitry to buffer its analog input signal and to provide zero and gain adjustments so that the A/D converter can provide a properly scaled digital output.

An eight channel DAC provides an adjustable elevation signal and a comparator threshold signal for each channel.

The digital outputs from the A/Ds are input to BGA1M and BGA1S for possible storage in the FIFOs. Parameters received via VMEbus determine whether A/D data is saved in the FIFOs and also the format of the saved data.

The readout of FIFO data is controlled by VMEbus signals received by BGA2. VMEbus information received by BGA2 is interpreted and then passed on to BGA1M and BGA1S when appropriate. In many cases, control parameters received by BGA2 are passed directly to BGA1M and BGA1S, but certain parameters are also retained by BGA2. For example, parameters such as digital thresholds, used only by BGA1M and BGA1S, are not retained.
by BGA2 whereas the mode parameter is stored in all thee FPGAs. Similarly, a parameter such as the board serial number is only stored in BGA2, since this parameter has no effect on the storage of A/D data by the other FPGAs.

2 Clocks

The VMEbus FPGA, BGA2, operates from a 50 MHz clock. BGA2 also sends this clock to BGA1M and BGA1S in order that those FPGAs can store parameters sent from BGA2. However, the primary clocks in BGA1M and BGA1S are 125 MHz, derived from the A/D converters. An externally supplied 500 MHz clock to the A/Ds is converted to 250 MHz output clocks for use in capturing digitized A/D values. BGA1M and BGA1S divide these clocks to 125 MHz, the phases of these clocks being adjustable to provide correct alignment for registering the A/D data.

3 Operating Modes of the WFD

The WFD can be operated in any of four modes, Test, Oscilloscope, Large Time Word and Fill and Time Word. In the Test mode, 64 bit test data may be written to and read from any FIFO using 64 bit VME block transfers.

The Oscilloscope mode is used to continuously collect sample data at a 500 MHz rate over an interval from receipt of a start signal to receipt of a stop signal. The start and stop signals can be issued as VME signals or as NIM start and stop inputs.

The Large Time Word and Fill and Time Word modes are almost identical. These modes store blocks of data but only when triggered by the data exceeding a certain level, determined either by an analog level sensor or by comparison of the digitized data with a digital threshold. As in the Oscilloscope mode, these modes only operate after a start signal has been issued and before a stop signal occurs. These modes store a trigger time (relative to the time of occurrence of the start signal) within each block of stored data. The Fill and Time Word mode differs from the Large Time Word mode in that the Large Time Word mode stores a 32 bit time value (indicating nanoseconds) whereas The Fill and Time Word mode stores a 16 bit time value plus a fill count. The fill count is the number of start-stop signal pairs issued after a fill reset has been issued.
4 General Operating Principles of the WFD

When power is first applied to the WFD, the three FPGAs are loaded with configuration data from a reprogrammable PROM after which the FPGAs become operational in their initial states with the VME FPGA, BGA2, waiting for commands from VMEbus and BGA1M and BGA1S waiting for commands from BGA2. After VMEbus commands have set the many control parameters, a start signal from a NIM input or a VMEbus command starts the data-collecting process in the selected operating mode. Digitized data in the FIFOs can be read by VMEbus while data collecting is in progress, but most parameters can only be changed while the WFD is in its stopped condition.

The four channels operate more or less independently, each channel having its own setup parameters. However the operating mode is the same for all channels. Channels may be enabled or disabled independent of one another. For the triggered modes (Large Time Word or Fill and Time Word), a trigger originating in one channel can be enabled to cause data storage in that channel or in any or all of the other channels.

Several conditions, such as a full FIFO, can be enabled to cause a VMEbus interrupt.

5 VME64x

The VME interface for the WFD follows the VME64x specification. This specification allows address relocation so that the address assignments for FIFO data are independent of the VME slot location. This specification also provides a control status register area, CSR area, where all of the WFD control parameters are located. A configuration ROM space is also provided, this space holding fixed information specifying the way VMEbus communicates with the WFD.

6 Data Transfers

VMEbus data transfers use a 32 bit data bus plus a 31 bit address bus. Block transfers use both the data bus and the address bus for 64 bit data transfers.

Data transfers between BGA2 and BGA1M and BGA1S occurs over two 8-bit bidirectional buses in conjunction with two 7-bit address buses and two
read and write signals. All setup parameters use single byte transfers.

Data from the A/Ds is sent to BGA1M and BGA1S as 16 bits every 4 nS using a differential PECL signal format. PECL receivers in BGA1M and BGA1S convert these signals to single-ended format where they are latched by both the rising and falling edges of their respective 125 MHz clocks.

7 Using HSTL and DCI

All signals between FPGAs use DCI (digital controlled impedance) to minimize signal reflections. Many signals also follow the HSTL II standard, a standard that uses small voltage transitions centered about either 1.5V or (in the case of the WFD) 1.8V. HSTL II and DCI may be combined to give logic operating with small voltage transitions with known input and output termination impedances.

8 Bank Assignments

The IO connections of the FPGAs are assigned to eight different physical locations or banks, each of which can have certain HSTL and DCI properties. Since there are restrictions as to which HSTL and DCI properties can be resident in a particular bank, the bank IO assignments for the FPGAs have been carefully chosen to facilitate inter-FPGA signal connections while accommodating these restrictions.

9 Floor Planning

The Xilinx ISE software was unable to automatically place the logic of BGA1M and BGA1S, so a limited amount of manual placement was needed. In particular, the several DCMs (digital clock managers, or phase-locked loops) and the BUFGMUXs needed manual placement as also did the location of certain logic modules.