Writing Test Data from BGA1M and BGA1S

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This paper describes the procedure used in BGA1M and BGA1S for writing test data to a FIFO. Test data is written using block transfers from VMEbus while the WFD is in its stopped state.

The eight bytes of each block transfer are transmitted serially from BGA2 to BGA1M and BGA1S, the last byte being accompanied by a beg_end signal from BGA2. The beg_end signal triggers the write sequence as shown in the timing diagram of Fig.1. Fig. 2 shows the logic associated with the timing signals of Fig.1.

In Fig.1, write_fifo is a delayed version of beg_end in the 50 MHz domain that is synchronized to the 125 MHz domain by twr1, which is then clocked into twr2 and twr3 to create a single test_write trigger signal to the write logic. At the fall of beg_end, the last byte of data from BGA2 is latched so the complete 64 bits of data are now valid and stable within BGA1M and BGA1S and available for writing to a FIFO.

The test_write signal is one of several inputs to the trigger logic used for all writes to a FIFO. This signal causes a latch_write_count bit to be set, which in turn causes the write_count to be set to 2. For other types of write triggers, the write count may be set to other values. Once set to a non-zero value, the write_count is normally decremented at the 125 MHz rate until it reaches a value of zero. In addition to setting the write_count, the latch_write_count signal also causes the write-enable signal, wen_b, to the FIFO to go low, allowing data to be written to the FIFO on the rising edge of the FIFO write clock. This write-enable signal is cleared after the write_count has been decremented to 1.

While the write procedure is going through its sequence, the block data to be written is also being moved through the registers of the write logic shown in Fig. 2. Two latched multiplexers, mux_1 and mux_2, are registering
the block data using the MB and MC multiplexer inputs. The multiplexer selection signals, selmux12 and selmux12, determine whether the MB or MC inputs are latched; when test_write is high, the MB inputs are selected, otherwise the MC inputs are used. The other multiplexer inputs are used when writing triggered mode or oscilloscope mode data.

From Fig.1, the data flow can be traced from the latched multiplexers to the delay registers, to the DDR register and then to the FIFO. The DDR register is a special register that clocks input data from D0 when C0 rises and from D1 when C1 rises, hence is able to provide input data to a FIFO at a 250 MHz rate, the rate needed when writing DDR data to the FIFO. 

Note from Fig.1 that the data into the DDR register always has a full 8 nanoseconds (one clock cycle) of setup time before being clocked by the normal or inverted 125 MHz clock.

Also shown in Fig.1 is the FIFO write clock. This 125 MHz clock is adjusted so its rising and falling edges are centered within the FIFO data input windows. Note that the FIFO write enable signal goes high before the last falling edge of the FIFO write clock, but this does not prevent the writing of FIFO data as long as the write enable signal is true on the rising edge of the clock.

The data shown in Fig.2 is 16 bits wide except at the input to the DDR register, where a 4 bit time nibble is added, making the DDR (and FIFO) inputs 20 bits wide. When writing test data, the time nibble has no meaning and is set to 1’s.

When the write_count is an odd number, a count up signal occurs, causing the FIFO count and the total word count to be incremented. For the test write mode, the write_count has only one odd value, namely 1, for each block write operation.
Fig. 1 Signal timing for writing test data
Fig. 2 Logic for writing test data