Automatic DCM Reset

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Although DCM’s (digital clock managers) usually start operating correctly without being initially reset, there is no guarantee of this. Xilinx suggests that a reset pulse of at least three clock cycles width always be applied to each DCM at startup. A simple reset circuit, suggested by Xilinx, is shown in the figure. This amounts to a four bit shift register with FDS1 initially set and FD1, FD2 and FD3 initially cleared since these are the startup states for FDS and FD flip flops.

As can be seen from the timing waveforms, the circuit automatically generates a DCM reset pulse spanning the necessary three clock cycles.

All of the DCM’s in the WFD make use of this reset logic.
DCM reset logic and timing