Readout of the Word Count

William E. Earle

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Reading the word count to VMEbus requires that the three bytes of the word count first be read from BGA1M or BGA1s to BGA2. Two counters are used to perform this transfer, one in BGA2 that counts from 8 down to 0 and one in BGA1M or BGA1S that counts from seven down to 0.

Referring to the attached timing diagram, a VMEbus request for a word count causes the state to change from idle to count-0 and then to count-1. The only purpose of state count-0 is to set the counter in BGA2 to 8.

In state count-1 at a count of 8, BGA2 issues a read request, dreq, to BGA1M or BGA1S that causes the current word count to be stored in a register and the counter in BGA1M or BGA1S to be set to 7. Both the counter in BGA2 and the counter in BGA1M or BGA1S are then decremented down to 0, with count decoding used to output the appropriate data byte from BGA1M or BGA1S to BGA2 and to latch the data into a three-byte register in BGA2.

When the counter in BGA2 reaches a value of one, the complete three byte word count from BGA1M or BGA1S has been received by BGA2 and is output over VMEbus in conjunction with a request for DTACK to be generated. When DS0* and DS1* return high, the DTACK signal is deactivated and the state returns to idle.

Note that the readout process only uses the 50 MHz clock, the transfer of the word count from the 125MHz domain to the 50 MHz domain being a continual operation that is transparent to the readout process.
Timing for count readout