The Analog Circuitry of the MULAN VME Card

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1 General Theory of Operation

This paper describes the analog circuit for one channel of the MULAN VME card. The circuit is designed to accept a negative input signal of up to 2.0 V amplitude and to convert this signal to an eight-bit digital value using a scale factor of 8 mV/bit. The circuit also provides digitally settable discriminator and input offset levels, both also using the same scaling of 8 mV/Bit. Four potentiometers provide for zeroing the offsets of the input amplifier, the analog discriminator and the A/D converter and for setting the span so that an analog input of -2.0V gives an eight bit digital output of exactly 250, one bit per eight millivolts.

The A/D converter is a MAX106 having both positive and negative analog inputs. These inputs can be used in either a differential or single-ended mode, the latter being the mode for the present application. The external input signal, after being buffered and offset by a DC level from a DAC, is connected to the negative input of the A/D. The positive input of the A/D is used to zero-adjust the A/D and to receive a 125 MHz sine wave needed when adjusting the clock phases of the four channels. In normal operation, the sine wave is not present at the positive input, so this input serves mainly as a zero-adjust input.

Fig.1 shows the analog circuitry for one of the channels. P2 allows for a slight offset adjustment to correct for the offsets of the input amplifier and the discriminator. With both the elevation DAC, U2, and the threshold DAC, U3, set for zero output, the input to the positive input of the discriminator, U5, is +0.510 V. With no input signal, P2 is used to adjust the output of U1
so that the discriminator is at its switching point, effectively cancelling the input offsets of U1 AND U5. P2 is able to adjust the negative input to U5 from +0.458 V to +0.560 V.

With the threshold DAC set to 250 decimal, corresponding to the maximum signal input of -2.0 V, the positive input to U5 becomes -0.4861 V. Since this is a span of 0.9961 V, the gain of U1 must be adjusted, via P1, so that an input signal of -2.0 V also gives an output span from U1 of 0.9961 V. With the resistor values shown, this span can be adjusted from 0.9707 V to 1.02515 V. The adjustment procedure consists of adjusting P1, with an input signal of -2.0V, until the discriminator is at its switching point. The gain of U1 from its positive input to its output is now 1.9922.

Since U1 drives the A/D through a series resistor intended to match the input impedance of the A/D, the signal span at the A/D is divided by two, to 0.49805 V. This is not quite the 0.5 V span needed by the A/D using the internal reference, so an external, adjustable reference is used, P4 being the adjustment potentiometer. In addition, an A/D offset adjustment is provided via P3.

Note that all but four of the resistors have 1% tolerance. The other four resistors are 0.1% tolerance and should not be replaced with 1% resistors or the overall specification of 1% for the span and offset cannot be guaranteed.

Fig.2 shows the circuit that generates the common reference voltages of +2.400, -2.400 and -0.6944 that are used by each channel. This circuit uses a precision 3.000V reference having less than 0.1% error.

When the 125 MHz sine wave is applied to the A/D, the offset DAC, U2, should be set to 125 decimal so that the negative input to the MAX106 is at zero volts.

2 The Adjustment Procedure

- Threshold zero adjustment. With U2 and U3 set for zero output and with no signal input, adjust P2 until the discriminator U5 is at its switching point.

- Threshold gain adjustment. With U2 set for zero output, U3 with a decimal value of 250 and with a -2.0 V signal input through a 50 ohm resistor, adjust P1 until the discriminator is at its switching point.
- A/D zero adjustment. With U2 set for zero output and with no signal input, adjust P3 until the A/D output is centered about 00 hex.

- A/D span adjustment. With U2 set for zero output and with a -2.0 V signal input through a series 50 ohm resistor, adjust P4 until the A/D output is centered about FA hex.

Fig. 1 The analog circuit for each channel is designed to keep span and offset errors to 1% or less.
Fig. 2 Reference voltages common to the four channels.