VME Module using complete digitizer ASIC and FPGA back-end

Digitizer ASICs (digital T, Q out)

PMT in

Channel A
Channel B

Channel Buffer

"Level One" Buffer

Readout FIFO

Trigger Matching Logic

Trigger FIFO

Large FPGA (i.e. Xilinx Virtex 2)

VME Interface Module Control (smaller FPGA?)

Global Trigger