ATM-DB Status

• 30 new testers received
  – All 30 tested, working

• Automatic test software written
  – Test time per board ~10 minutes

• 30 new DB received
  – 5 tested as of today
    • All hardware features working
ATM-DB Hardware Plans

- Will send 5-10 testers with new ATM-DB to Japan on 1/15 with Aaron
- Most remaining boards from batch of 30 could be shipped by end of January
  - keep a few in Boston
ATM-DB Firmware

- New DB firmware written to match specification
  - Many changes from current test firmware
    - Byte order reversed to network order for all registers
    - New SDS start, stop, warning cells implemented
    - All register addresses changed
  - Includes all required features for Super-K operation
  - Testing started at BU
  - Tester firmware updated also to (partly) simulate ATM
  - Expect to have a version with most bugs fixed by end of January. May have a preliminary version sooner.

http://ohm.bu.edu/cgi-bin/superk
Many diagnostic counters added to ATM-DB firmware  
Should help in debugging and measuring performance (transfer rate)  
All are 64 bits and will not wrap around

<table>
<thead>
<tr>
<th>Address</th>
<th>r/w</th>
<th>bit(s)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>200-207</td>
<td>r</td>
<td>0-63</td>
<td>Number of words written to SDRAM FIFO</td>
</tr>
<tr>
<td>208-20f</td>
<td>r</td>
<td>0-63</td>
<td>Total number of words SDS read from ATM</td>
</tr>
<tr>
<td>210-217</td>
<td>r</td>
<td>0-63</td>
<td>Total number of SDS bursts</td>
</tr>
<tr>
<td>218-21f</td>
<td>r</td>
<td>0-63</td>
<td>Total number of words lost due to buffer full</td>
</tr>
<tr>
<td>220-227</td>
<td>r</td>
<td>0-63</td>
<td>Number of SDS bursts completely lost due to buffer full</td>
</tr>
<tr>
<td>228-22f</td>
<td>r</td>
<td>0-63</td>
<td>Number of SDS bursts partially lost due to buffer full</td>
</tr>
<tr>
<td>230-23f</td>
<td>r</td>
<td>-</td>
<td>reserved, read all as 00</td>
</tr>
<tr>
<td>240-247</td>
<td>r</td>
<td>0-63</td>
<td>Number of words in SDRAM FIFO</td>
</tr>
<tr>
<td>248-24f</td>
<td>r</td>
<td>0-63</td>
<td>Time SDRAM is empty from first write to SiTCP last write (40 ns units)</td>
</tr>
<tr>
<td>250-257</td>
<td>r</td>
<td>0-63</td>
<td>Time TX_FIFO_AFULL is high from first write to last SiTCP to last write (40 ns units)</td>
</tr>
<tr>
<td>258-25f</td>
<td>r</td>
<td>0-63</td>
<td>Total time elapsed from first write to SiTCP to last write (40 ns units)</td>
</tr>
<tr>
<td>260-267</td>
<td>r</td>
<td>0-63</td>
<td>Total TCP connection time (40 ns units)</td>
</tr>
<tr>
<td>268-26f</td>
<td>r</td>
<td>0-63</td>
<td>Total time with TCP_ESTABLISH=1 and TX_FIFO_AFULL=0</td>
</tr>
<tr>
<td>270-277</td>
<td>r</td>
<td>0-63</td>
<td>Total number of bytes written to SiTCP</td>
</tr>
<tr>
<td>278-27f</td>
<td>r</td>
<td>0-63</td>
<td>Total number of errors detected on pseudo-random data written to SiTCP</td>
</tr>
</tbody>
</table>
Firmware Testing Status

- Simple tests completed using updated ATM-DB Ethernet library (J. Raaf). Large amounts of pseudo-random test data can be read and verified in “memory test” mode
- Detailed testing of SDS features just starting
Tester Firmware Features

- TKO bus test (can read back last, F, SA, D)
- SDS with simulated data:
  - Sequential (counter) data
  - Pseudo-random (LFSR) data
  - Data from FIFO
- SDS control
  - SDSREQ, G_Trig signals (fixed or random interval)
  - Length can be fixed, random or infinite
    - Random values can be limited to programmable $2^N$ maximum
Tester Features (Continued)

- **SPI interface simulation**
  - Responds to SPI RDID instruction as M25P32 flash

- **Test signals available for logic analyzer/scope:**
  - SPI (SCK, CSn, S0, SI)
  - TKO (SDSREQ, G_Trig, TKOCLK, DOIT*)
Production Test
(work by J. Raaf)

- **Test procedure for new boards:**
  - Power up, check supply voltage, current
  - Program CPLD, FPGA with JTAG cable
  - Connect via Ethernet, program flash sectors
  - Check switches (with operator help)
  - Check FPGA status, SSN
  - SDRAM/data test (pseudo-random data check)
  - Dump all test results to database

- **Takes ~10 minutes/board (not optimized):**
  - Less than 1 month for 1 person to test 600 boards
Testing / Commissioning ATM-DB

• Propose to meet in Kashiwa April or May:
  – Test new DB with new ATM (hardware compatibility)
  – System tests with multiple ATM-DB and trigger/DAQ

• Further tests as more of system becomes ready
  – Test as possible in Boston using tester
  – Fix firmware bugs, add features as needed
DAQ Test in July 2007

- Requirements for this test:
  - Almost all existing ATM-DB and testers in Japan
  - New ATM-DB firmware debugged
  - Tester firmware requirements for this test defined and implemented

- Further discussion required about what is needed to support this test