Ethernet Daughterboard

Status Report

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Current Status

- **SiTCP working on our DB**
  - Helpful interaction with Uchida-san to fix bug
- **Firmware/software to download FPGA flash over Ethernet exists***
- **Firmware for TKO bus master control via ethernet ready**
- **3 working DB and 2 working tester**
  - Could send a setup to Uchida-san if needed

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* As of writing, there is a problem with lost UDP packets which prevents flash programming from working. Hopefully this will be fixed in the next days

Eric Hazen
Goals for Integration

• Mate DB with ATM, ensure power supplies and basic operation are OK
• Test TKO read/write of registers
• Test data readout of ATM events
  – Check that data is correct
  – Measure performance
• Test for pickup noise from DB
• Anything else?
What is Needed?

- **Hardware**: ATM, DB, Tester, Laptop
- **DB firmware**
  - Simple TKO access using UDP
  - Block transfer using TCP
- **Software**
  - UDP/TCP Ethernet tests [done]
  - Simple TKO access [J. Raaf, S. Wu]
  - ATM readout [J. Raaf and ???]
- **Hardware/firmware/software problems?**
  - All necessary software, tools, experts should be available during testing
More details

• Simple software will be provided by BU
  - However, details of ATM readout require some help of Japanese colleagues
  - We can define a C/C++ interface to read/write to TKO to build on
  - Jen should start a dialog with the appropriate collaborator who is familiar with the ATM and how it is read out over TKO
More details

• During the testing, we need experts available to help with:

  – ATM issues:
    • Hardware design (schematics and someone who can read them)
    • Firmware design (ability to get changes made if needed)
    • Software to read out ATM over TKO bus
  – General computer/network support
  – DB issues:
    • Hardware, firmware, software can be handled by Eric and Jen (on site) or Wu (e-mail)
JTAG/FPGA programming

• FPGA can be programmed via JTAG signals from ATM (or our tester)
  – This is opposite of what was specified-- ATM is supposed to be controlled by DB JTAG
    • Will fix in next version if needed

• FPGA can be initialized from flash at power-up

• Flash is programmed via Ethernet only (not JTAG compatible)
Backup Slides
Prototype Ethernet Daughterboard

- XC3S1500 FPGA
- SDRAM 32MB DDR
- Switches
- Ethernet PHY
- Ethernet Transformer
- CPLD
- Flash Memory
- Voltage Regulators
- Connector to ATM
- Connector to ATM
Ethernet DB Tester

Spartan 3 FPGA

60MHz Oscillator

Tester JTAG

DB RS-232

RS-232 DB Connector

Ethernet Connector
Daughterboard Tester

Spartan 3 FPGA

TKO Bus 34
JTAG 4
60Mhz Clock

1.2V, 2.5V, 3.3V, 5.2V Voltage Regulators

Power Conn

Daughterboard Site

RJ-45 conn

15V

LEDs

RS-232

DB-9 Conn

JTAG conn

Flash Mem

1.2V
2.5V
3.3V

1.2V, 2.5V, 3.3V, 5.2V

RS-232 DB-9 Conn

Flash Mem

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

RJ-45 conn

DB-9 Conn

RS-232

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

RJ-45 conn

Flash Mem

1.2V
2.5V
3.3V

1.2V, 2.5V, 3.3V, 5.2V

Flash Mem

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

RJ-45 conn

Flash Mem

1.2V
2.5V
3.3V

1.2V, 2.5V, 3.3V, 5.2V

Flash Mem

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

RJ-45 conn

Flash Mem

1.2V
2.5V
3.3V

1.2V, 2.5V, 3.3V, 5.2V

Flash Mem

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

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Flash Mem

1.2V
2.5V
3.3V

1.2V, 2.5V, 3.3V, 5.2V

Flash Mem

LEDs

Test conn

RS-232

DB-9 Conn

LEDs

RJ-45 conn